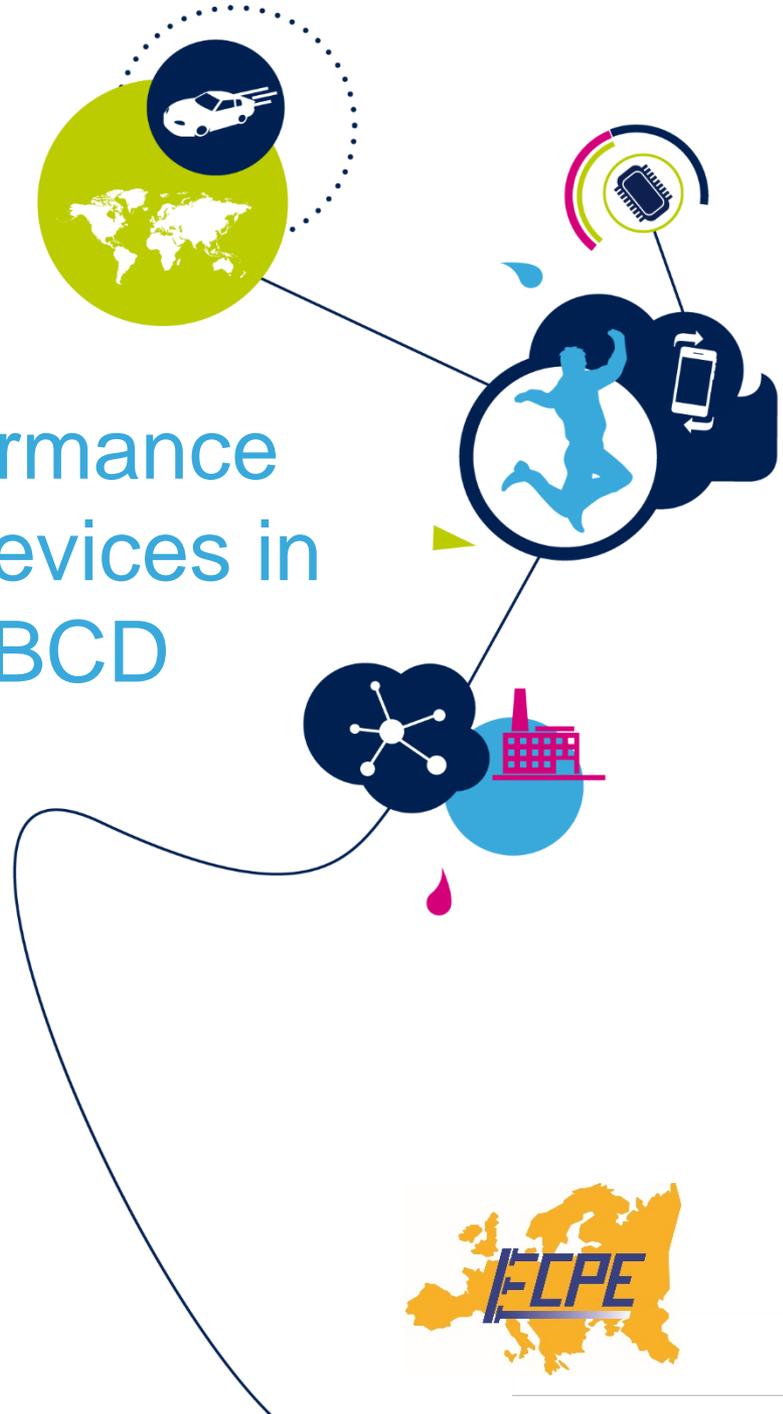


# Integration of High Performance Robust Lateral DMOS Devices in Advanced Smart Power BCD Platform

R. Depetro<sup>1</sup>, G. Croce<sup>1</sup>, P. Galbiati<sup>1</sup>,  
A. Tallarico<sup>2</sup>, S. Reggiani<sup>2</sup>, F. Giuliano<sup>2</sup>, C. Fiegna<sup>2</sup>

<sup>1</sup> Technology R&D, STMicroelectronics, Agrate Brianza, Italy

<sup>2</sup> ARCES-DEI, University of Bologna, Cesena, Italy



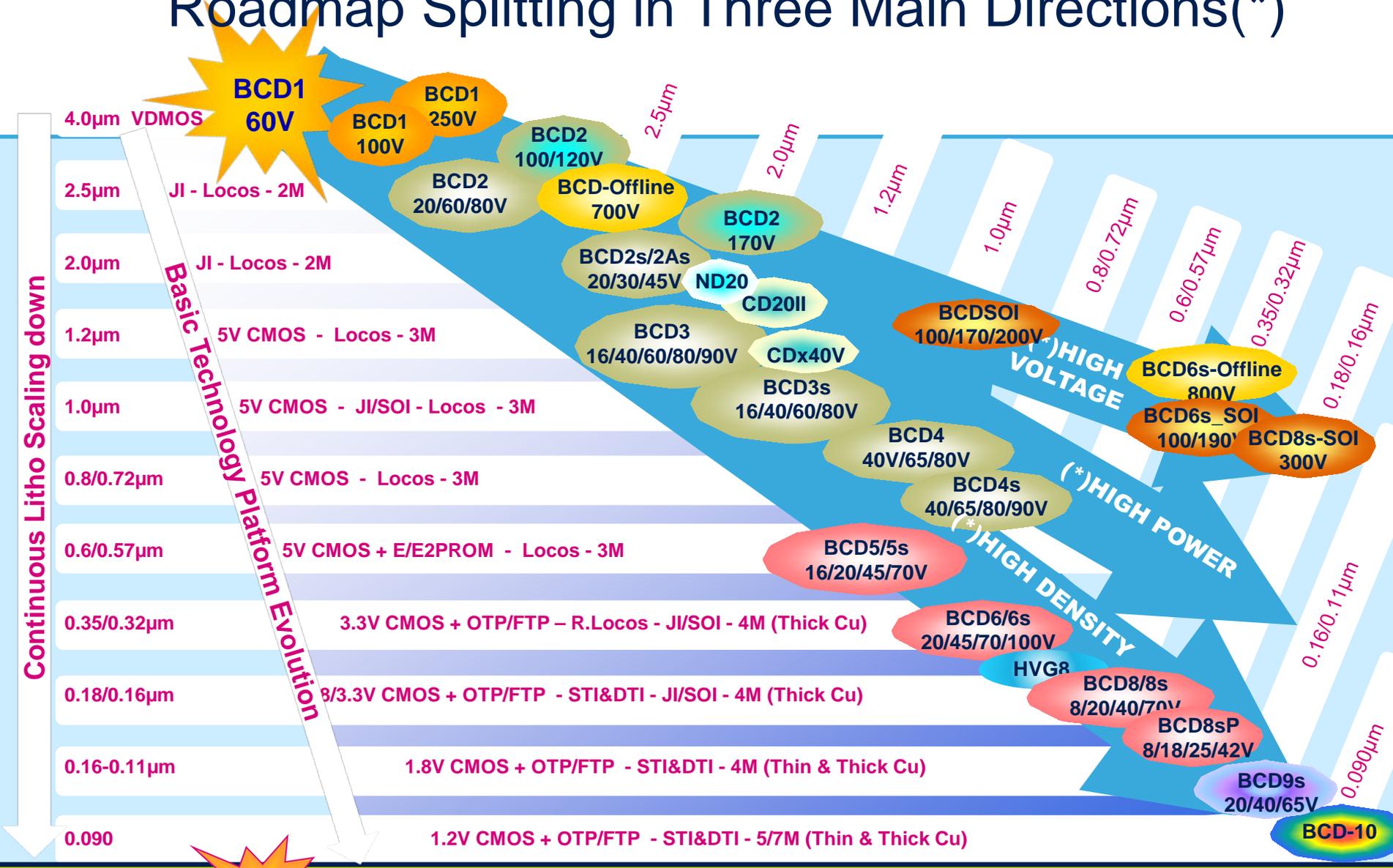
- History and evolution
- Where and what robustness count
- How (to try) to address problems ...
- Examples
- Conclusions

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# BCD Technology Segmentation

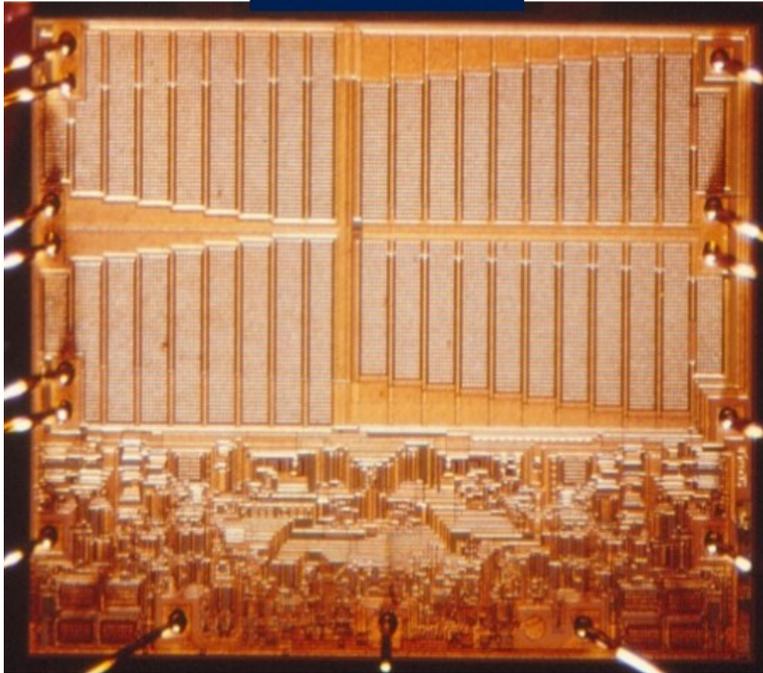
SEGMENT	TECHNOLOGY PLATFORM	APPLICATION FIELDS	
High Voltage BCD	0.32µm <b>BCD6s Offline</b> 3.3V / 5V CMOS – 25V/800V/1200V	 Lighting  Motors  Electrical Car	
	<b>BCD6s HV Transformer</b> 3.3V CMOS - Galvanic Isolation 4-6KV		
SOI BCD	<b>SOI-BCD6s</b> 3.3V CMOS - 20V/50V/100V/190V	 Full digital amplifier  Echography  AMOLED  Pico-projector	
	<b>SOI-BCD8s</b> 1.8V CMOS - 70V/100V/140V/200V		
Advanced BCD	0.16µm <b>BCD8sP - 0.16µm</b> 1.8V CMOS - 10V/18V/27V/42V/60V	 HDD  Airbag  Power Line modems  Audio amplifier	
	<b>BCD8sAUTO - 0.16µm</b> 3.3V CMOS - 20V/40V/65V/100V		
	0.11µm <b>BCD9s - 0.11µm</b> 1.8V CMOS - 10V/40V/60V		
			<b>BCD9sL - 0.11µm</b> 3.3V CMOS - 20V/40V/65V/100V
			<b>BCD9sE - 0.11µm – ePCM</b> 1.8V CMOS - 10V/40V/60V
	90nm <b>BCD10 - 90nm - ePCM</b> 1.2V CMOS - 8V/20V/40V/65V		 Printers  ABS  Power Supply  Automotive  ESP  Power Management for Mobile

# “More Than Moore” BCD Diversification Roadmap Splitting in Three Main Directions(\*)



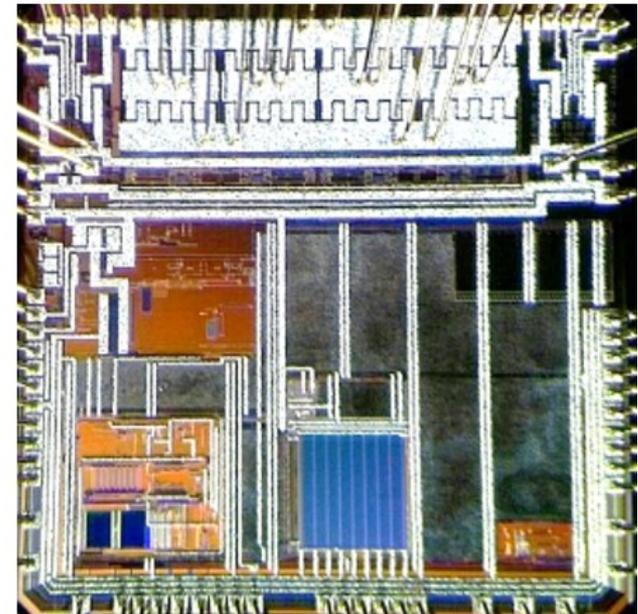
# What Does This Evolution Mean?

BCD1  
4000nm  
1000 Transistors



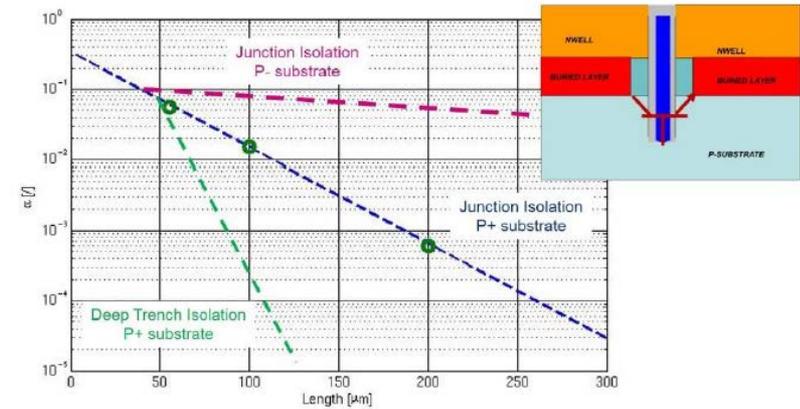
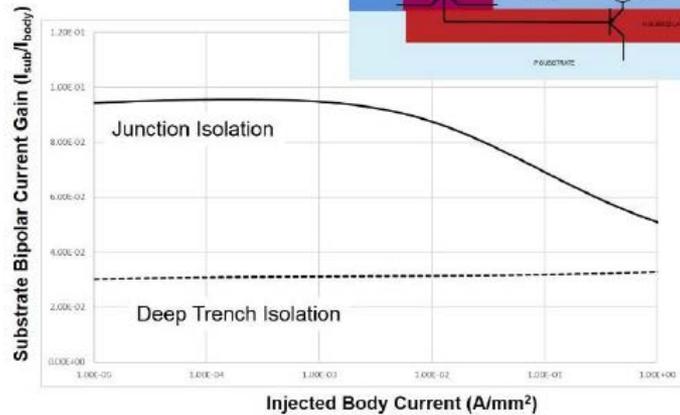
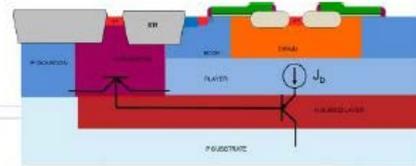
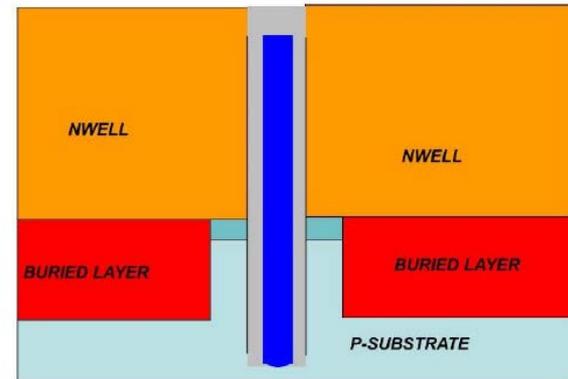
2x Half-bridges

BCD9s e-PCM  
110nm  
1 Million Transistors

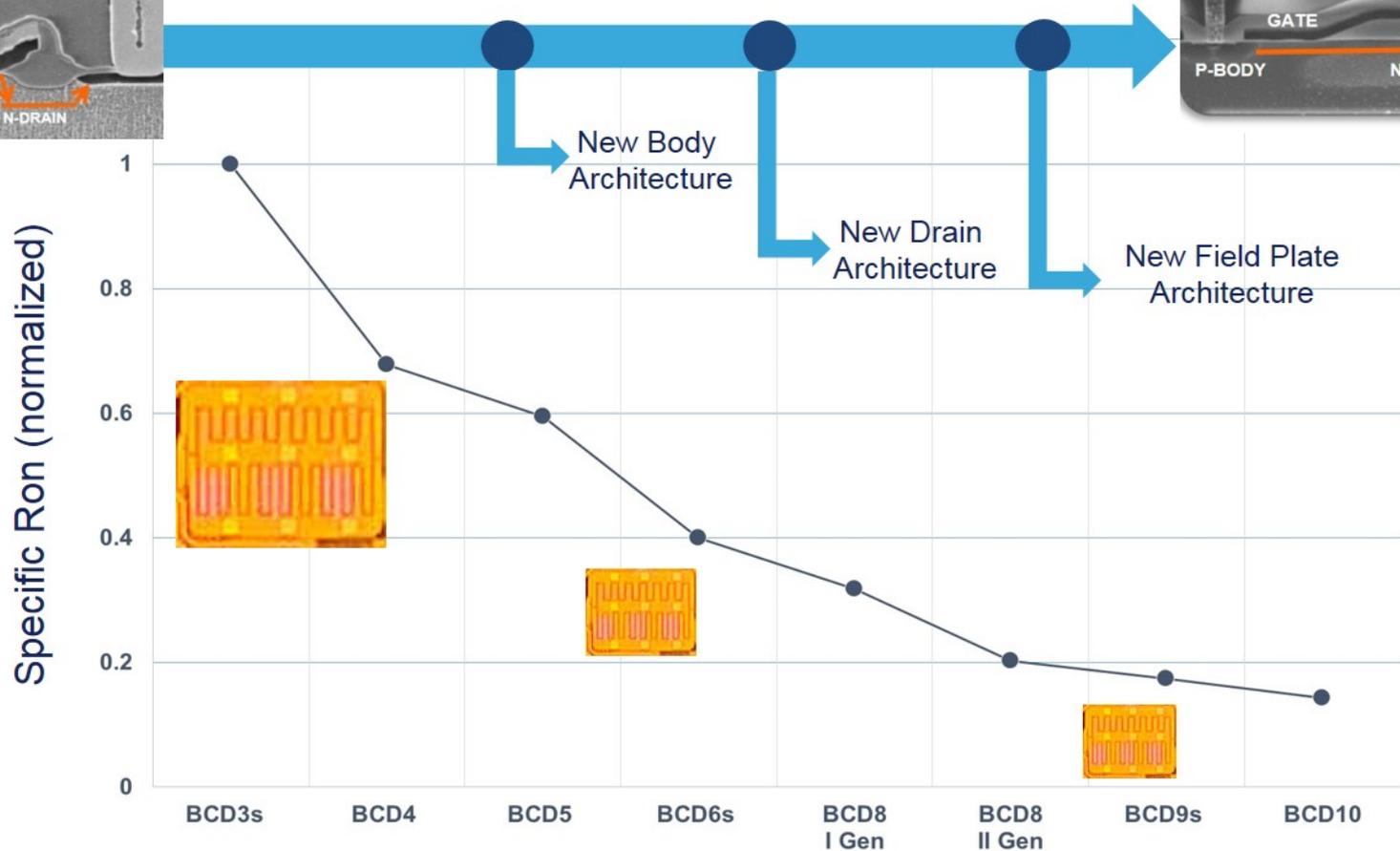
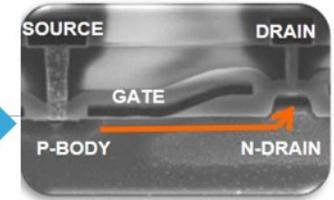
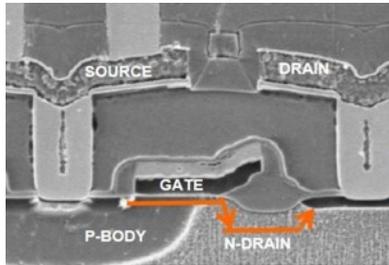


4x Half-Bridges  
8x 40V gate drivers ARM Cortex-M4  
32KB ePCM and 8KB RAM  
2x DACs and 1x ADC

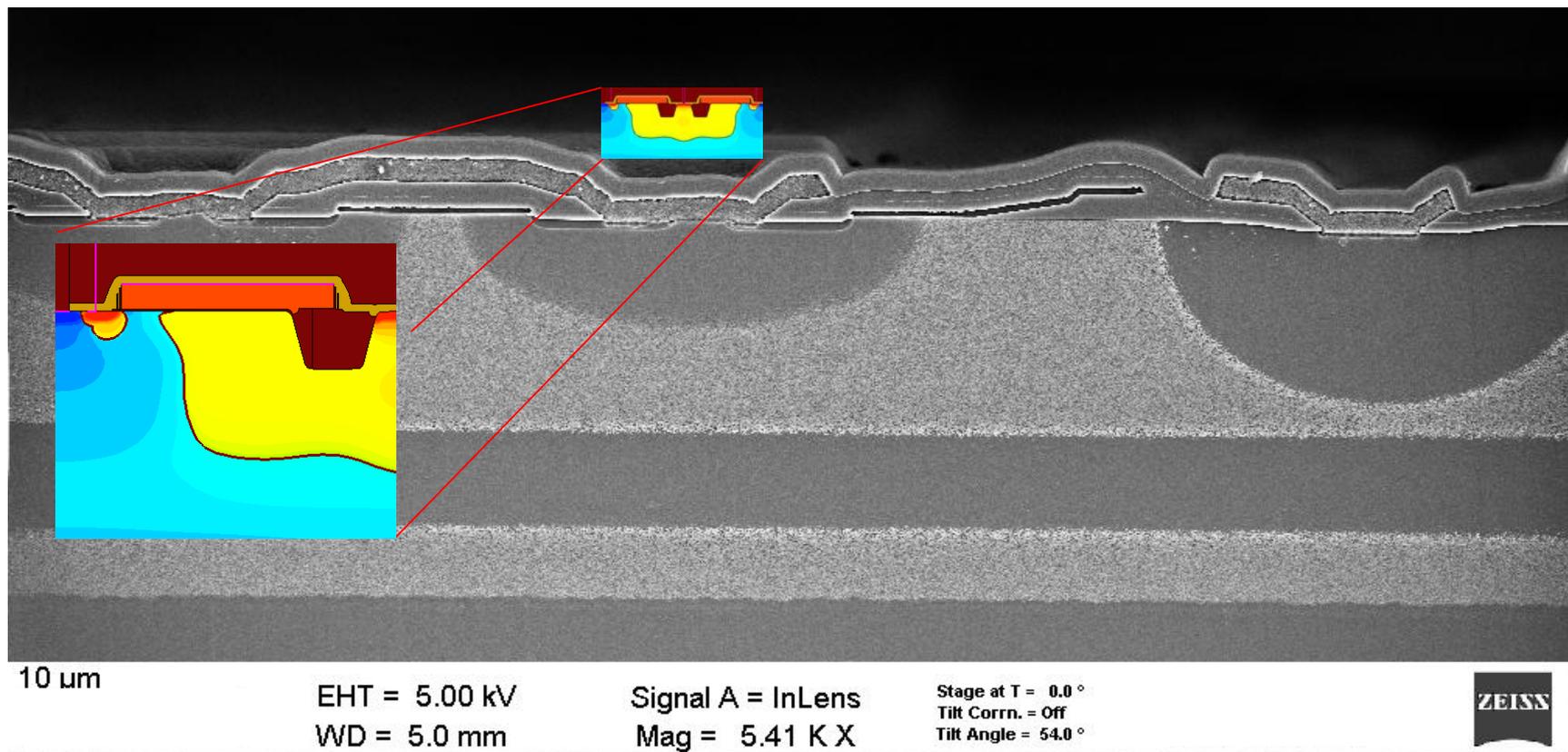
# Robustness in the Integration



# How to Continue to Improve on HV Devices

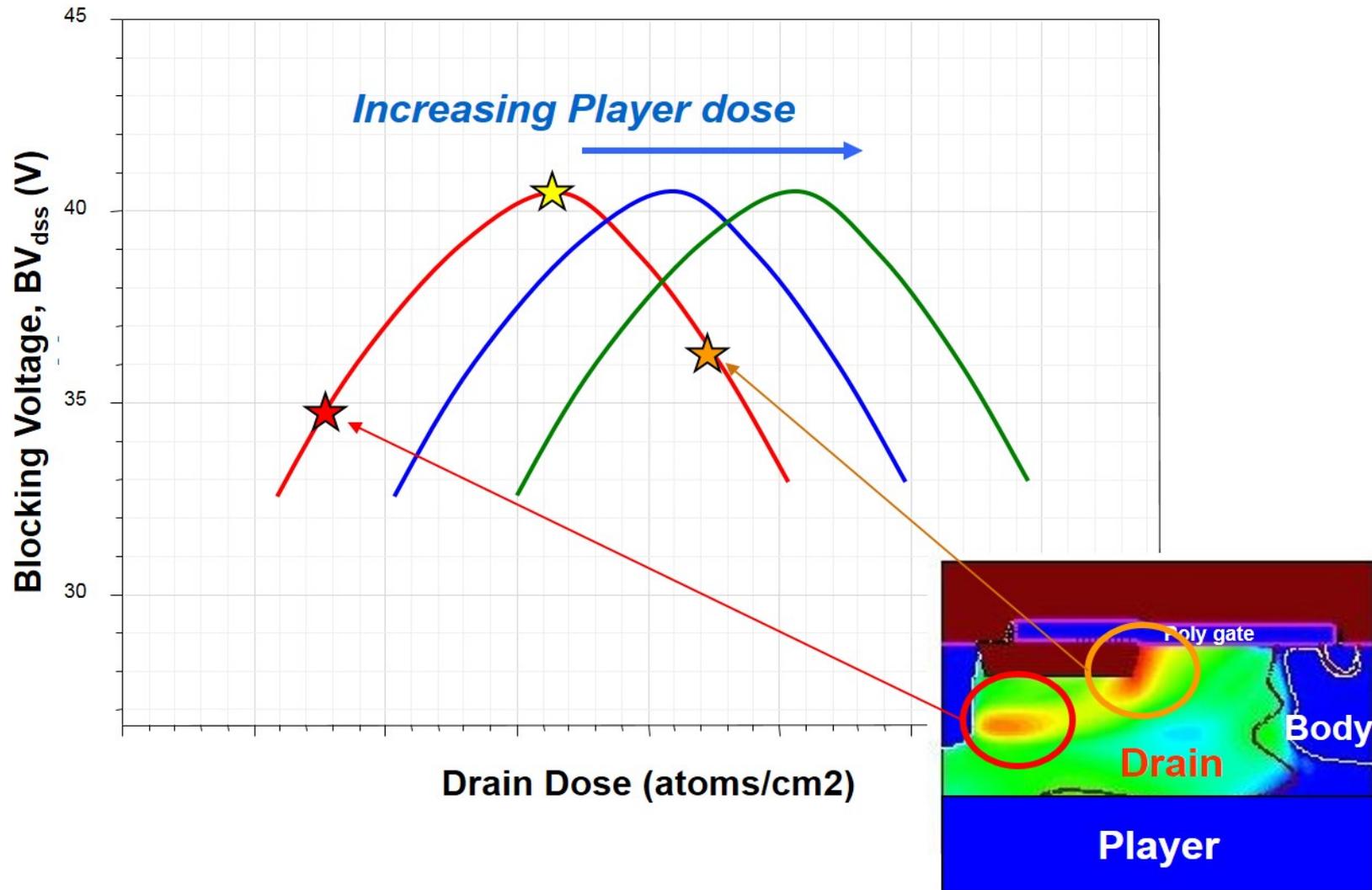


# Tapered oxide usage evolution from BCD I to BCD 10

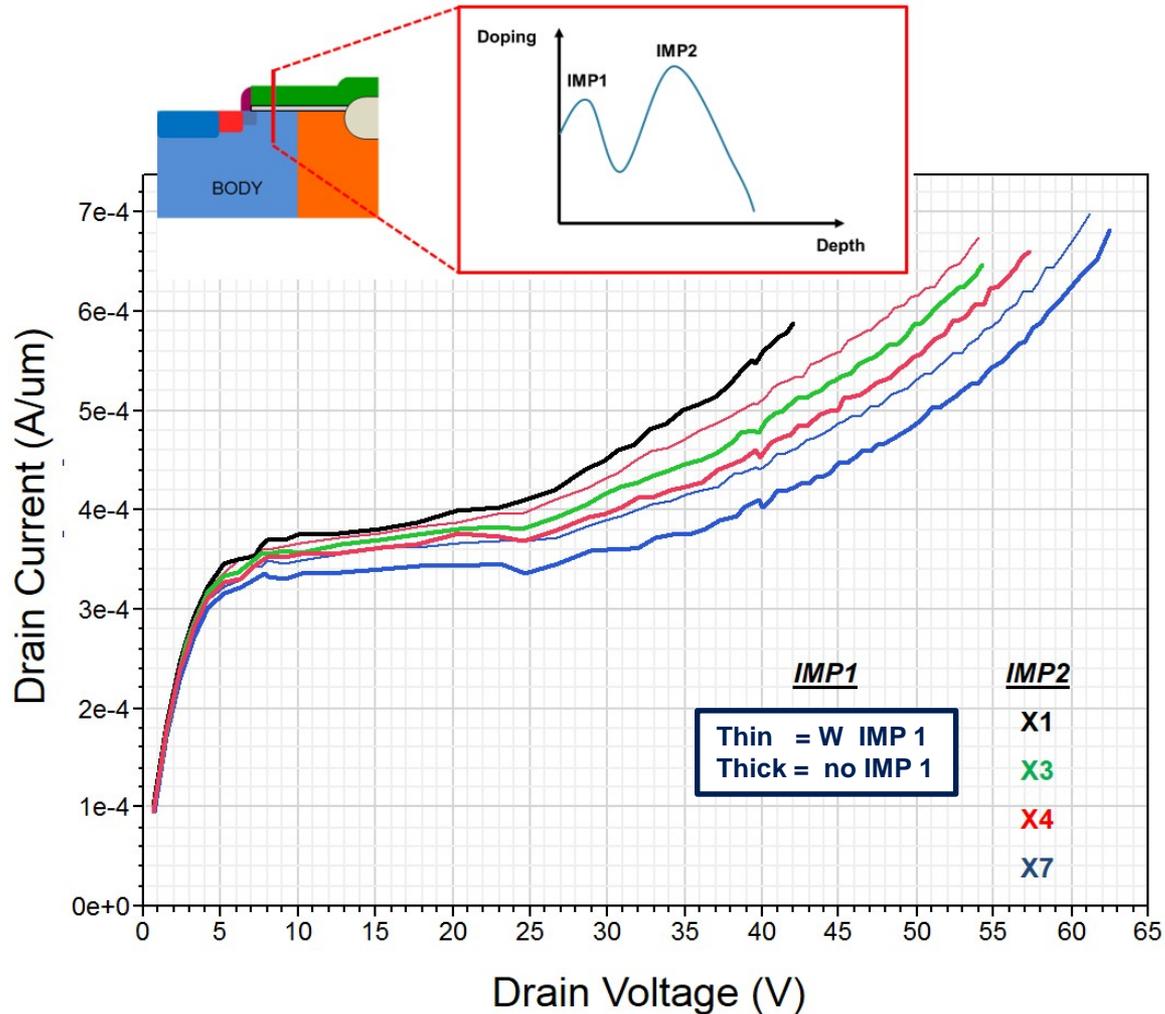


- History and evolution
- Where and what robustness count
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# Double RESURF Exploitation

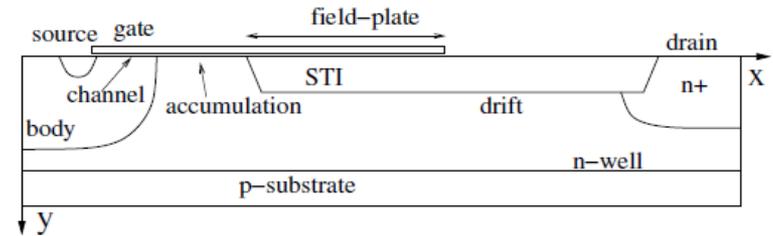
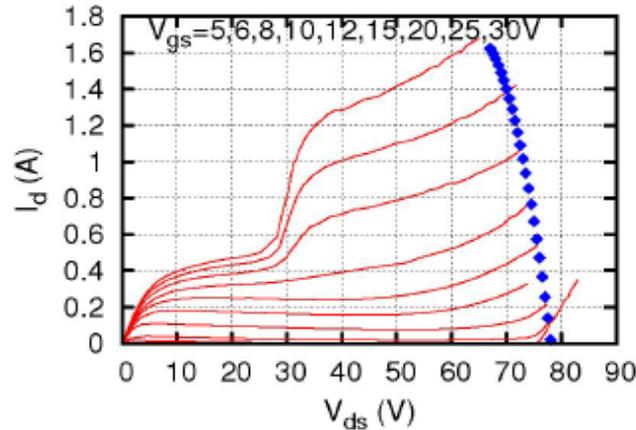


# Safe Operating Area and Body Doping



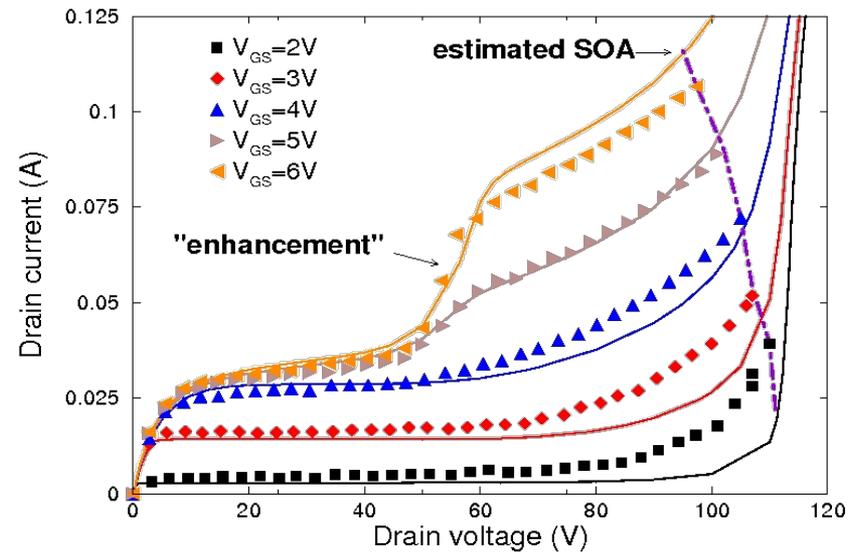
# Having Wide SOA

J. Lin et al., ISPSD 2006

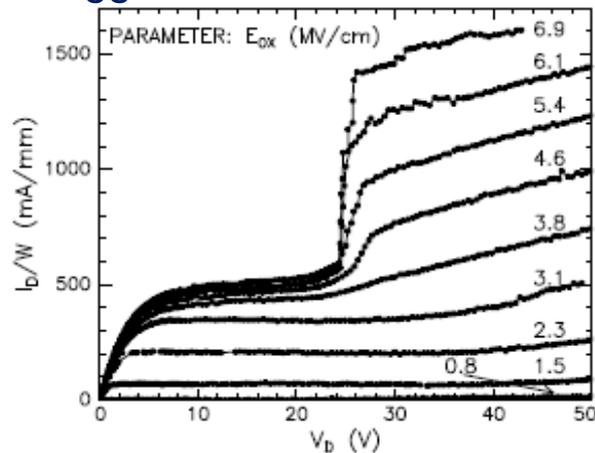


S. Reggiani et al., IEEE TED 2009

lines: simulations; symbols: experiments

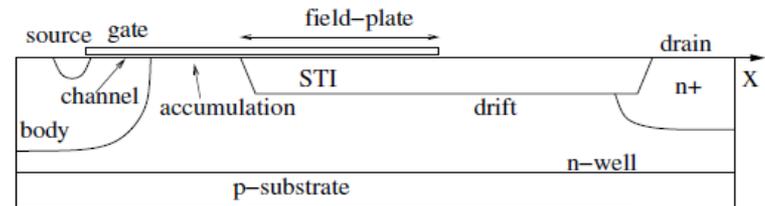


R. Roggero et al., ISPSD 2013



# Having Wide SOA

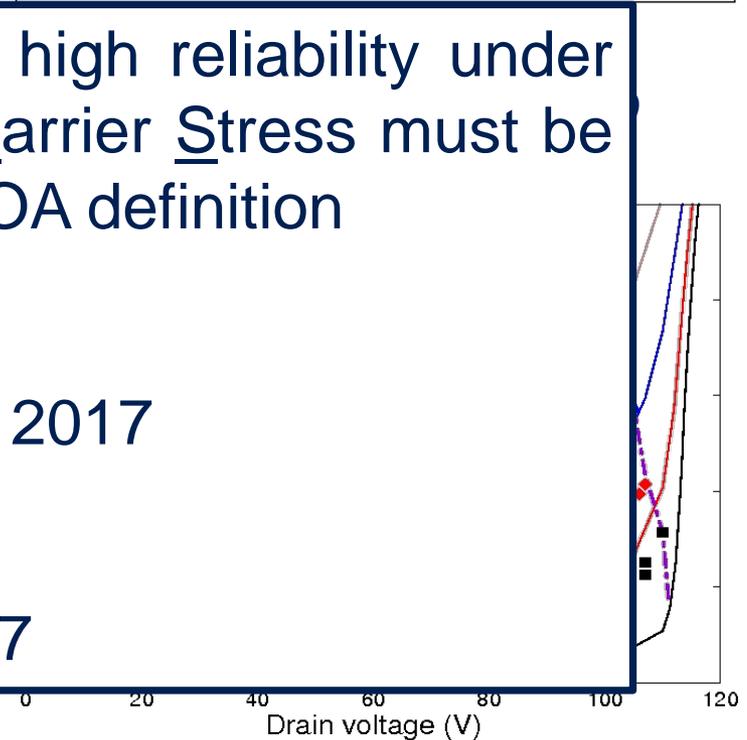
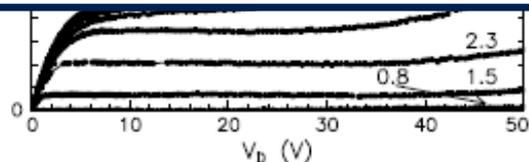
J. Lin et al., ISPSD 2006



Robust devices need also high reliability under stressing conditions: Hot Carrier Stress must be taken into account in the SOA definition

- J. Hao et al., IRPS 2016
- S. Liu et al., TED August 2017
- F. Jin et al., ISPSD 2017
- T. Mori et al., ISPSD 2017

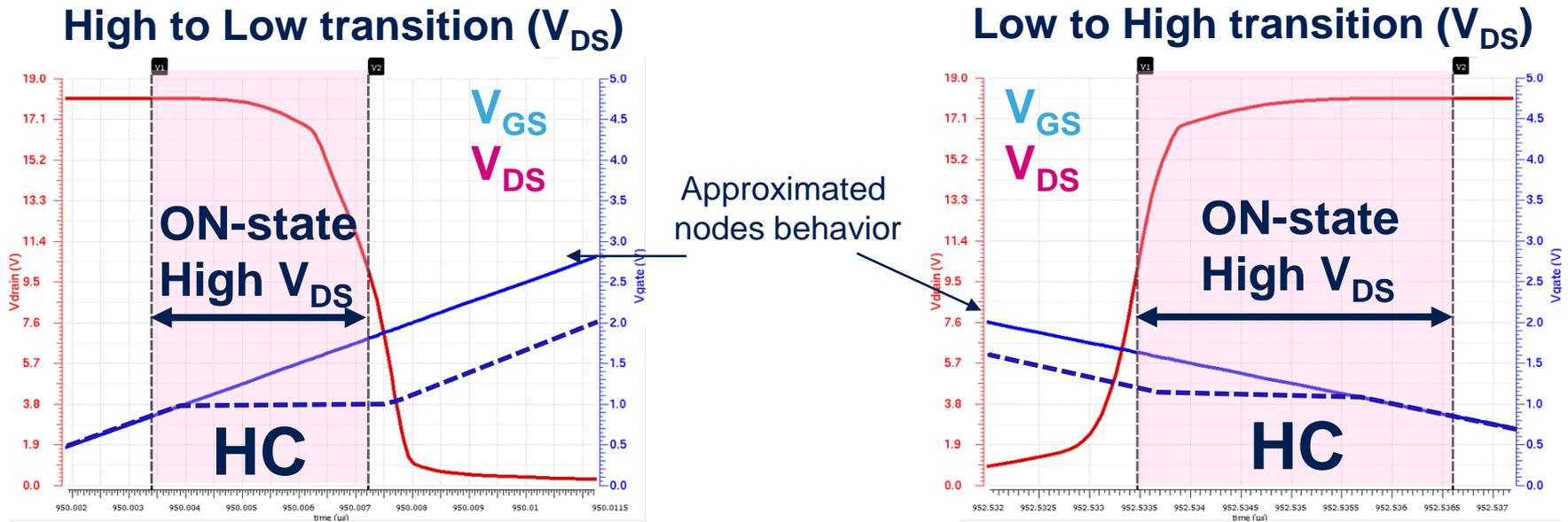
R.



- LDMOS device working condition is generally limited by degradation of
  - Maximum linear current ( $|\Delta I_{d,lin}| = \Delta R_{on}$ ) for high  $V_{DS}$  and low  $V_{GS}$  (standard working conditions in switching applications)
  - Threshold voltage ( $\Delta V_t$ ) for high  $V_{DS}$  and high  $V_{GS}$  (more related to spikes)

# When Degradation Occurs

- HC degradation in a real application: Switching phase

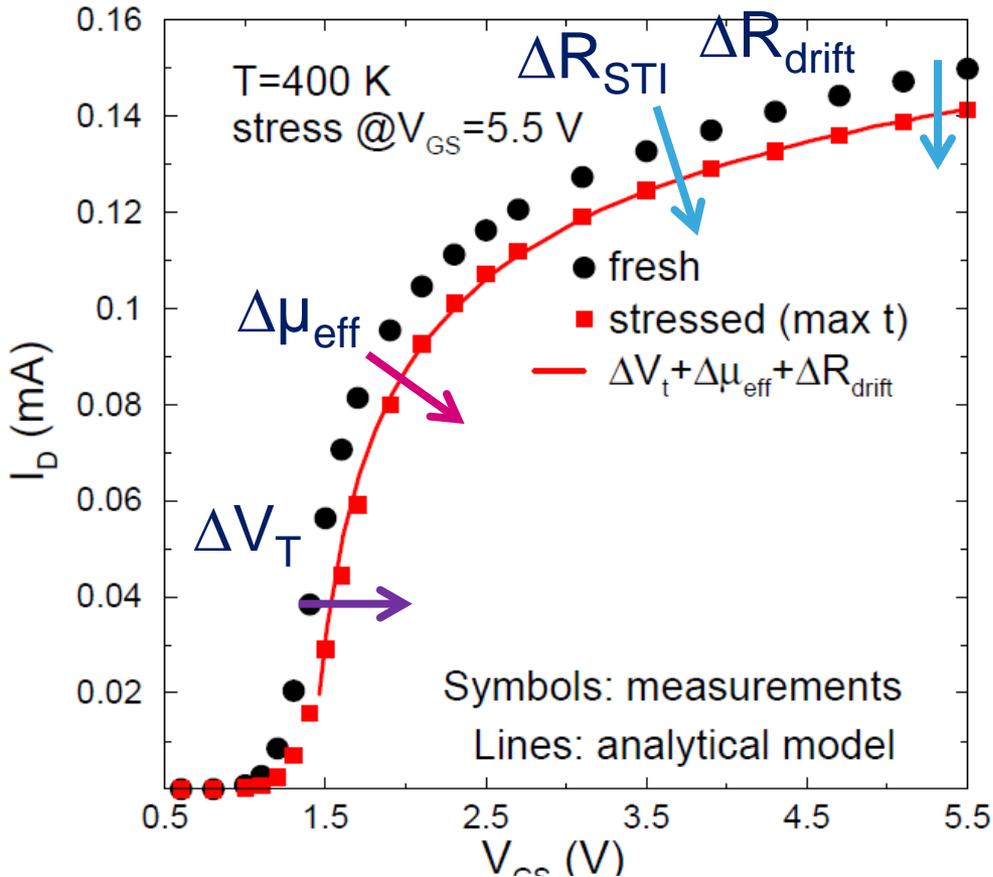


- History and evolution
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# The Design Tool-kit for the Total SOA

- Technology Computer Aided Design (TCAD) commercial tools for process and device simulations
  - Device simulation approach
    - 2D domain
    - Poisson + drift-diffusion transport equations
    - Impact-ionization accurate model
  - ... But TCAD is now helpful to quantitatively predict the HCS (Hot Carriers Stress) degradation induced by defects generated at the Si/SiO<sub>2</sub> interface!
- **HCS degradation model**

# HCS Degradation Analysis on the Localization

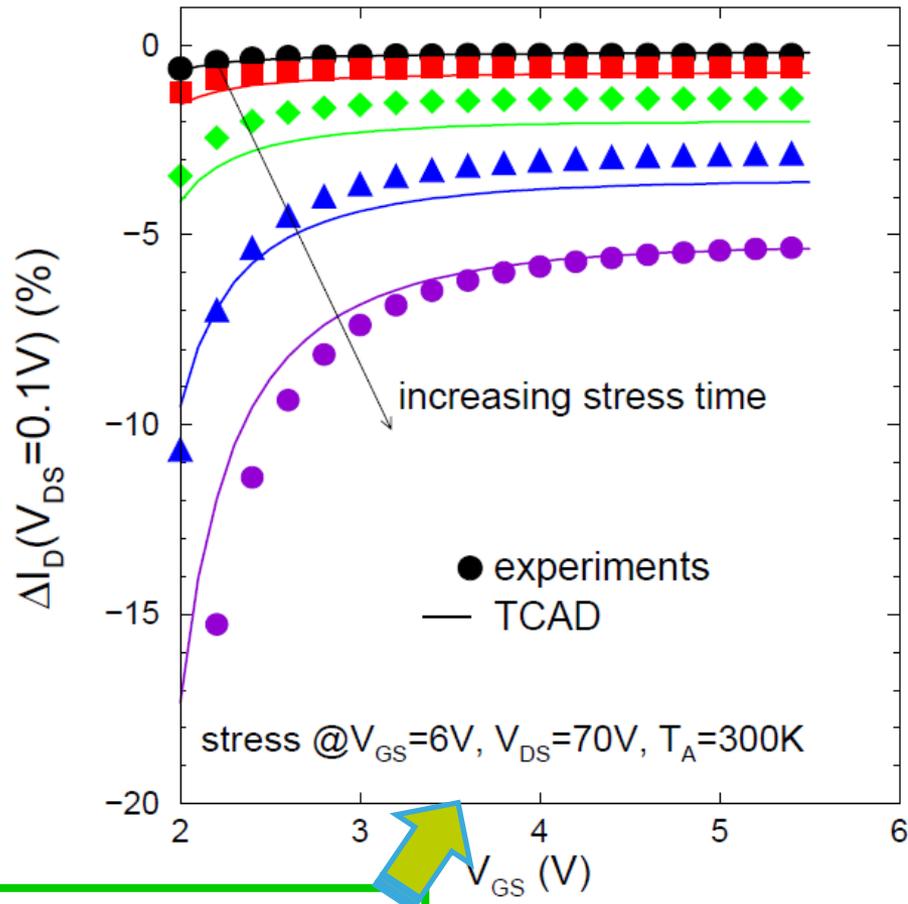
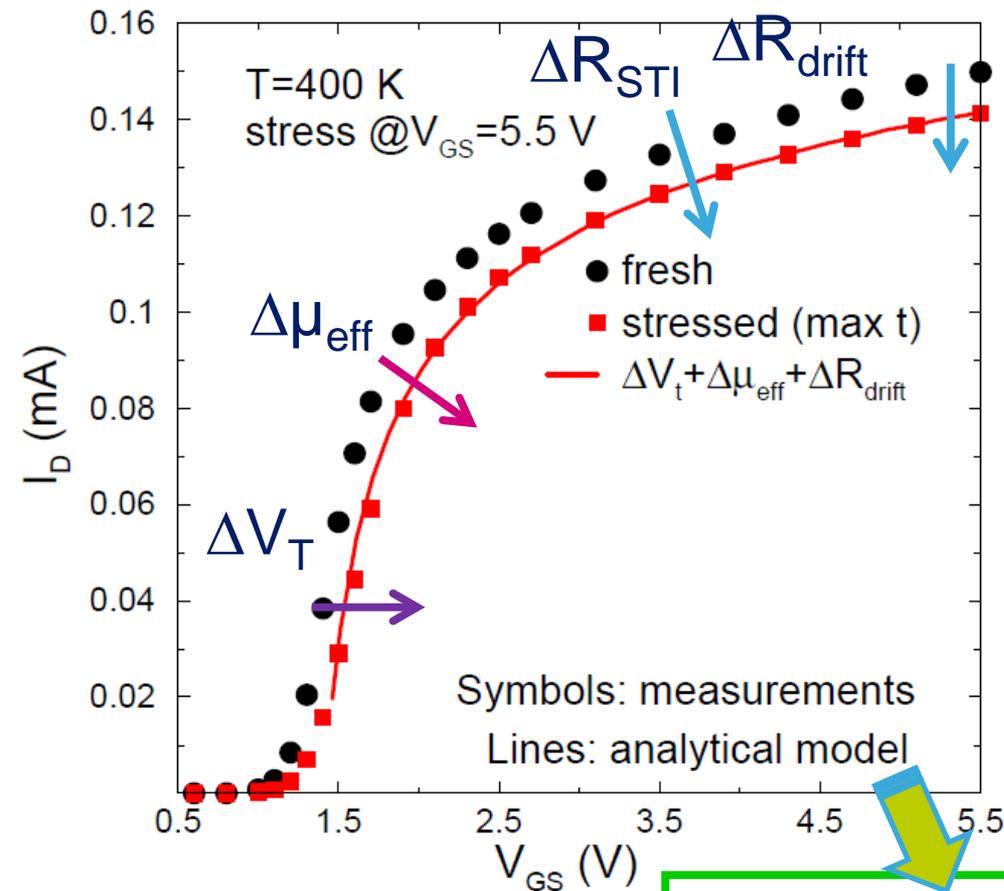


1. Trap formation in the **channel**  
→  $V_T$  shift ( $\Delta V_T$  in  $R_{ch}$ )
2. Trap formation in the **channel**  
→ **effective mobility** reduction ( $\Delta \mu_{eff}$  in  $R_{ch}$ )
3. Trap formation in the **drift**  
→ **drift resistance** increase ( $\Delta R_{STI}$  and  $\Delta R_{drift}$ )

The different dependences on  $V_{GS}$  are used to check the localization of degradation.

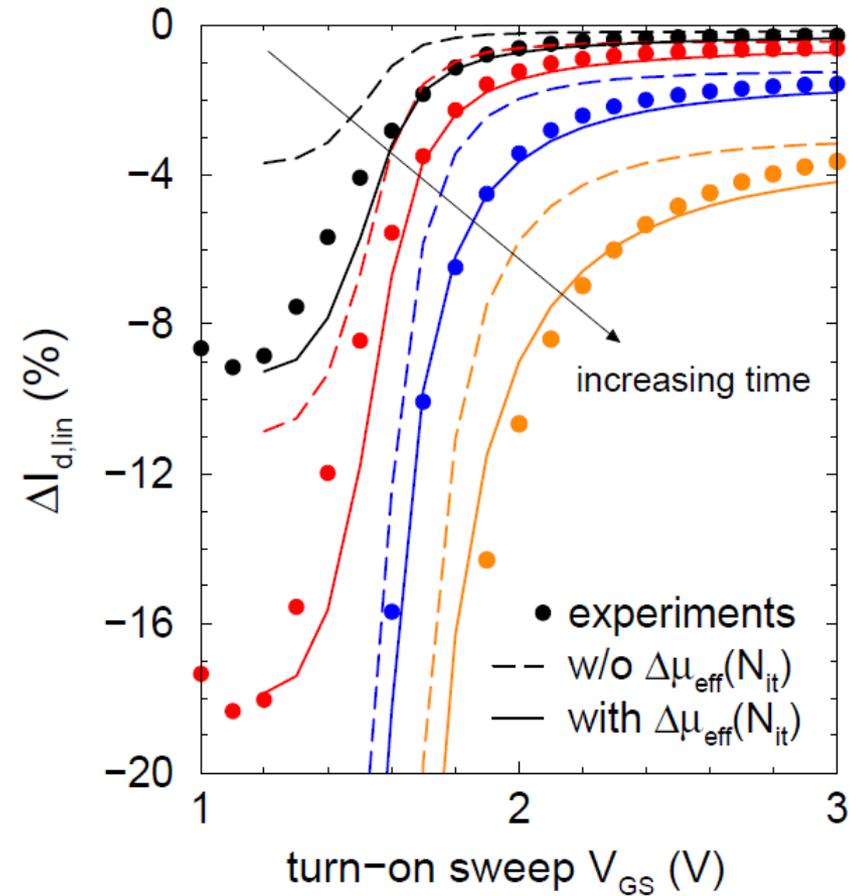
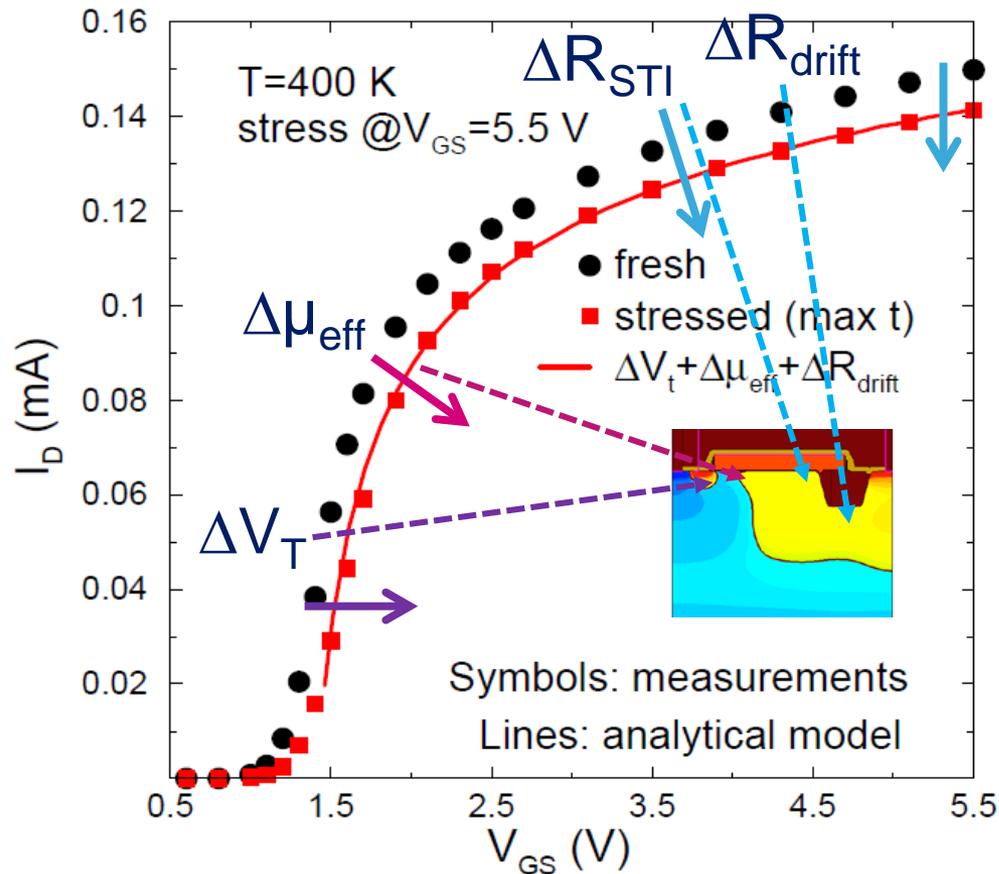
S. Reggiani et al., IEEE TED 2011

# Degradation Along Turn-on Sweep

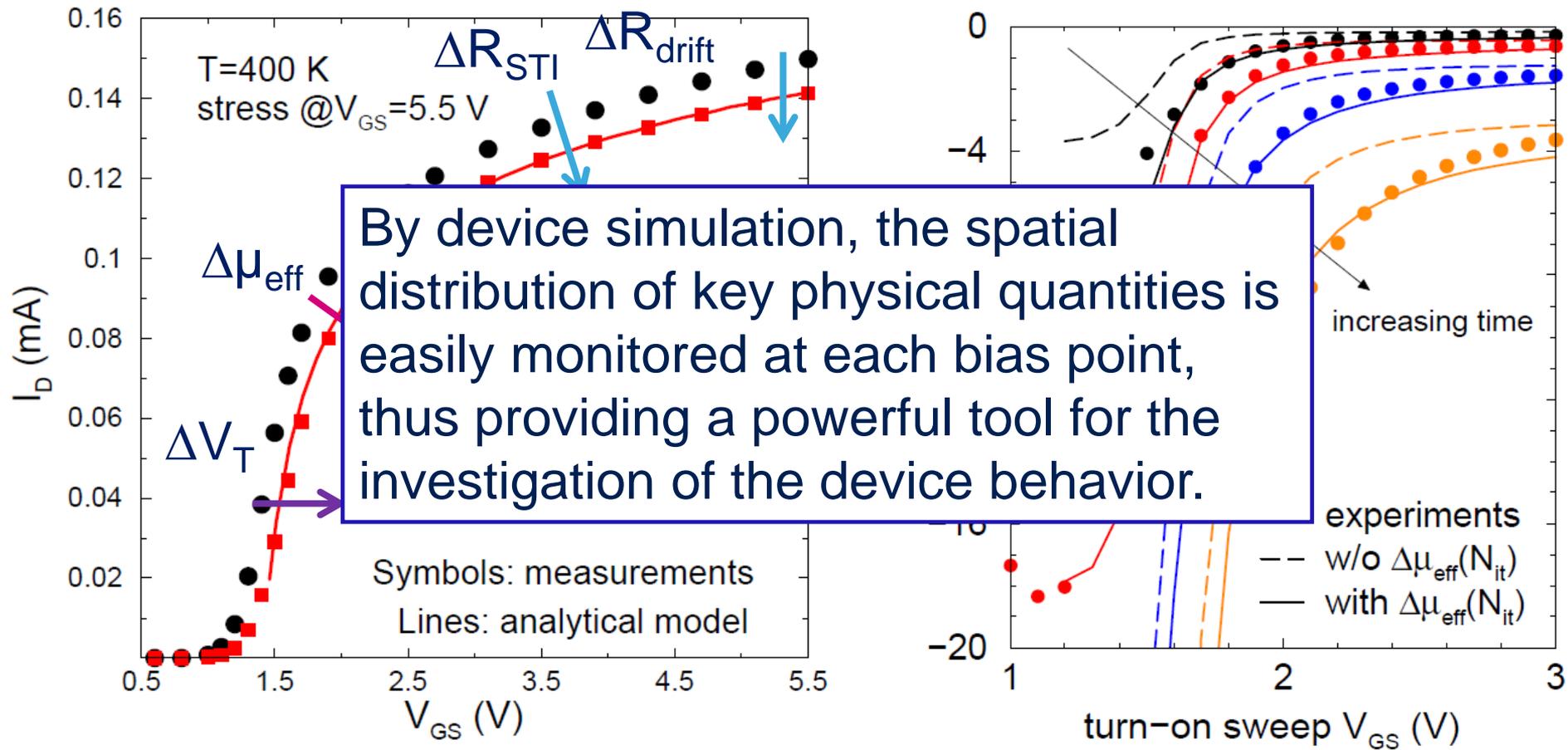


$$\frac{\Delta I_D}{I_D}(V_{GS}) = \frac{I_D(V_{GS}) - I_D^0(V_{GS})}{I_D^0(V_{GS})}$$

S. Reggiani et al., IEEE TED 2011



S. Reggiani et al., IEEE TED 2011



S. Reggiani et al., IEEE TED 2011

# Kinetic Equations of the Trap Generation: 1

Single-particle process (SP)

$$N_{it,SP}(\mathbf{r}, t, E_{SP}) = P_{SP} N_0 [1 - e^{-k_{SP}(\mathbf{r}, E_{SP})t}]$$

$\infty$

$P_{SP}$ : probability for SP generation

$$k_{SP}(\mathbf{r}, E_{SP}) = \int_{E_{SP}}^{\infty} f(\mathbf{r}, E) g(E) v(E) \sigma_{SP}(E) dE$$

$f(\mathbf{r}, E)$  - distribution function       $g(E)$  - density of states       $v(E)$  - group velocity

**3.1eV** [S. Tyaginov, MR 2010; K. Hess et al., IEDM 2000]

**11** [I.A. Starkov et al., J. Vac. Sci. Technol. B, 2011]

$$\sigma_{SP}(E) = \sigma_{SP0} \left( \frac{E - E_{SP}}{k_B T} \right)^{P_{SP}}$$

Cross-section models the electronic excitation, the expected normalization to  $k_B T$  was added [S. Reggiani, TED 2013]

$\sigma_{SP0}$ : fitting parameter

# Kinetic Equations of the Trap Generation: 2

$$N_{it,MP}(\mathbf{r}, t, E_{MP}) = P_{MP} N_0 \left[ \frac{P_{emi}}{P_{pass}} \left( \frac{P_u}{P_d} \right)^{N_1} (1 - e^{-P_{emi}t}) \right]^{1/2}$$

Fitting parameters

- $P_{MP}$ : probability for MP generation
- $\nu_{emi/pass}$ : emission/passivation frequency;
- $E_{pass}$ : passivation energy

Excitation induced by incoming electrons (multiple-vibrational electron-phonon interaction)

$$k_{MP}(\mathbf{r}, E_{MP}) = \int_{E_{MP}}^{\infty} f(\mathbf{r}, E) g(E) \nu(E) \sigma_{MP}(E) dE$$

$E_{ph} = 0,25 \text{ eV}$  [I.A. Starkov et al., J. Vac. Sci. Technol. B, 2011]

$$\sigma_{MP}(E) = \sigma_{MP0} \left( \frac{E - E_{MP}}{k_B T} \right)^{P_{MP}}$$

**0.1** [I.A. Starkov et al., J. Vac. Sci. Technol. B, 2011]

$\sigma_{MP0}$ : fitting parameter

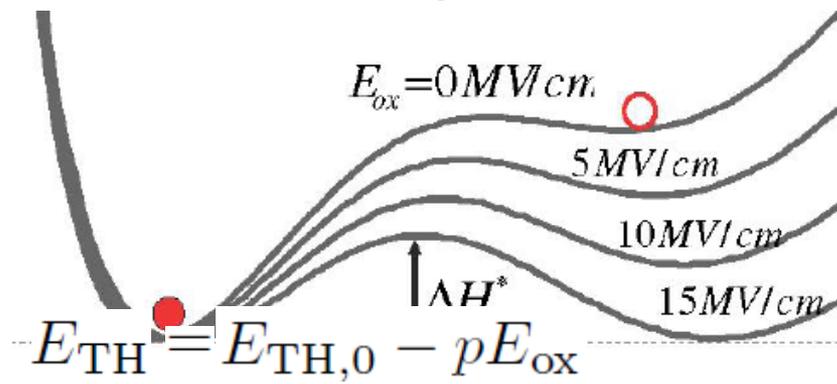
# Kinetic Equations of the Trap Generation: 3

Thermally-activated dielectric degradation (TH)

$$N_{it,TH}(\mathbf{r}, t, E_{TH}) = P_{TH} N_0 [1 - e^{-k_{TH}(E_{TH})t}] \quad \leftarrow [S. Reggiani, TED 2013]$$

$P_{MP}$ : probability for TH generation

Field-induced dipolar effect:



$$k_{TH}(E_{TH}) = \nu_{TH} \exp \left[ -\frac{E_{TH}}{k_B T} \right]$$

$\nu_{TH}$ : lattice collision frequency

J.W. McPherson et al., J. Appl. Phys. 88, 2000

- The physics-based models for the reaction rates need a **semiclassical transport solution** → numerical solution of the full-band Boltzmann Transport Equation (BTE) for the determination of the electron distribution function

...implemented in TCAD!

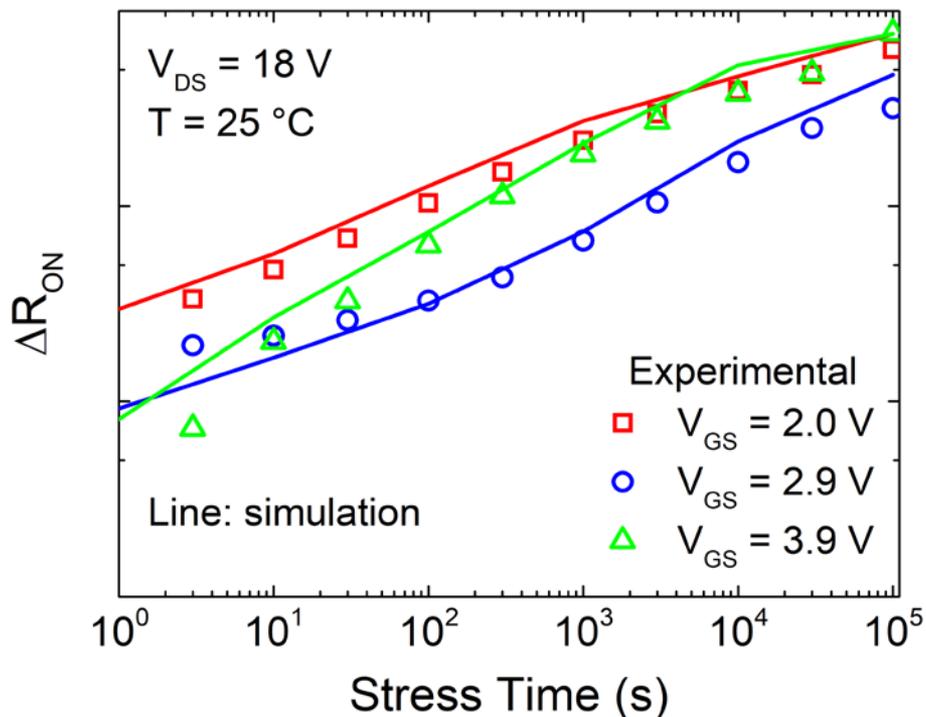
- Deterministic solution the spherical-harmonics expansion of the BTE
- Full-band structure obtained from the nonlocal empirical pseudopotential method.

**Accurate description  
of  $f(x,y,E)$  up to 10 eV**

S. Jin et al.(SISPAD 2009) - implemented in SDevice-Synopsys

- History and evolution
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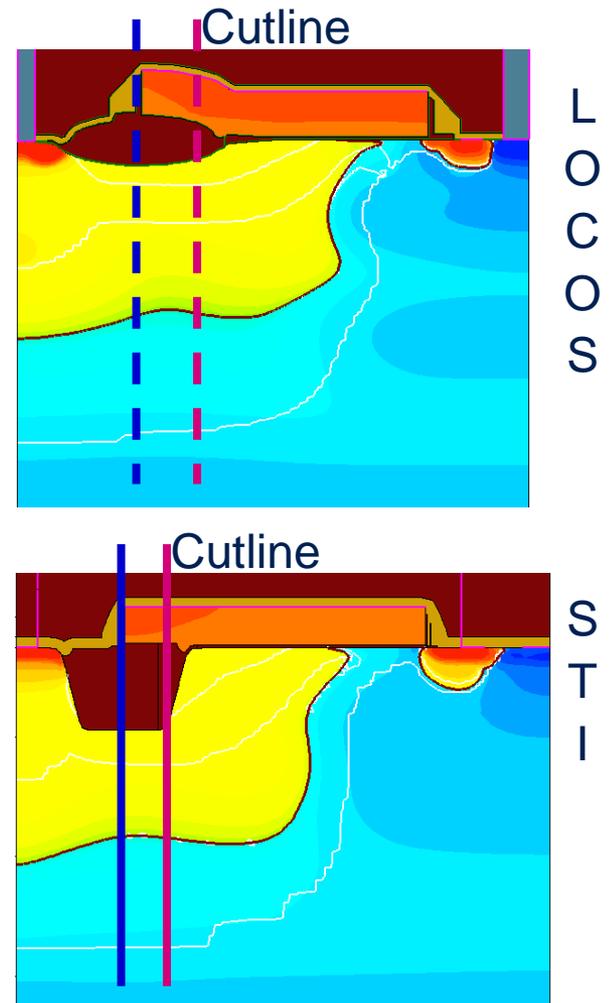
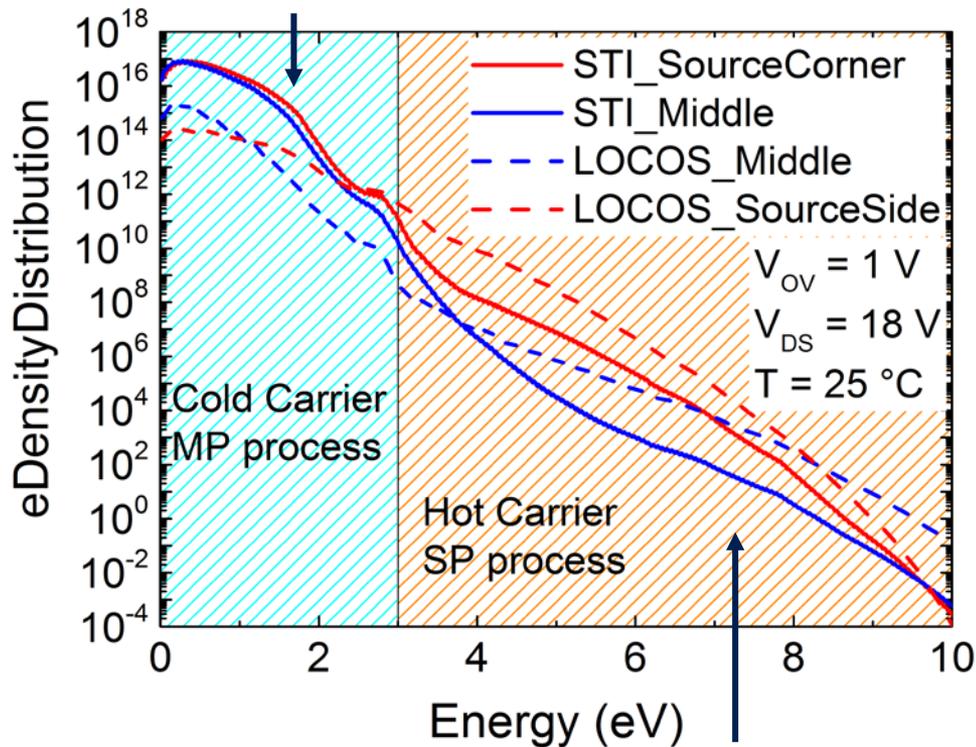
- Single- and Multiple-particle processes accounted for in the simulation



- Experimental  $\Delta R_{ON}$  and its gate bias dependence are reproduced by means of TCAD simulation
- Model calibration (SP and MP) is required to better fit the short stress times

# Electron Density Distribution (LOCOS vs STI)

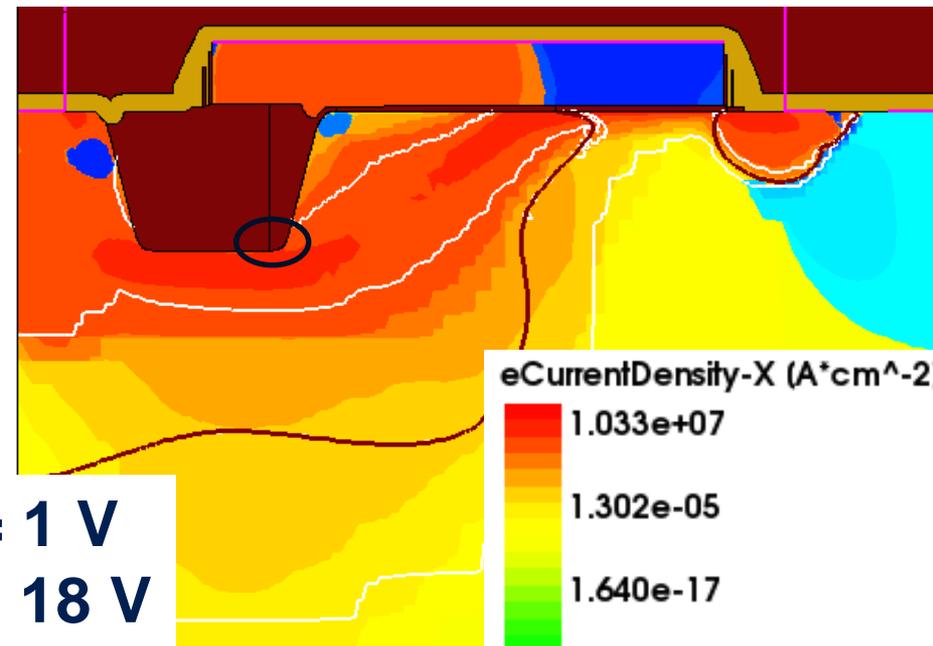
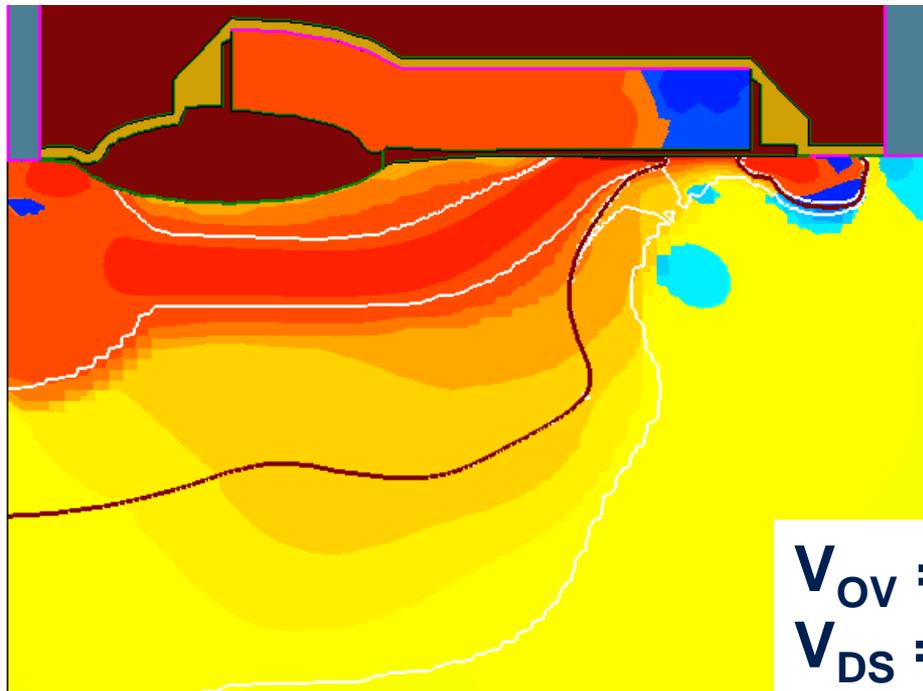
- A higher number of electrons may lead to higher number of interface traps in the STI structure due to **multiple-particle process**



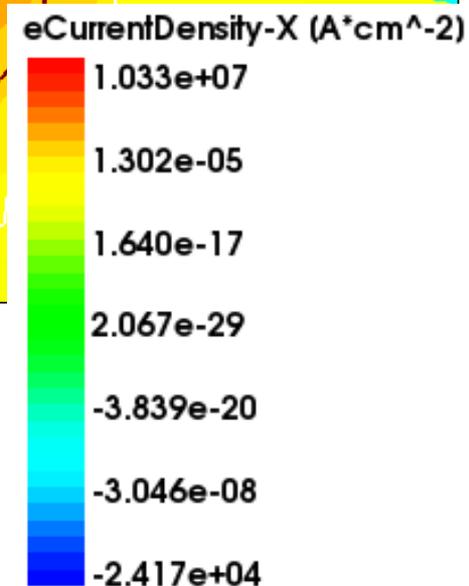
- **Single-particle** may be worse in LOCOS

## Selective LOCOS

## STI



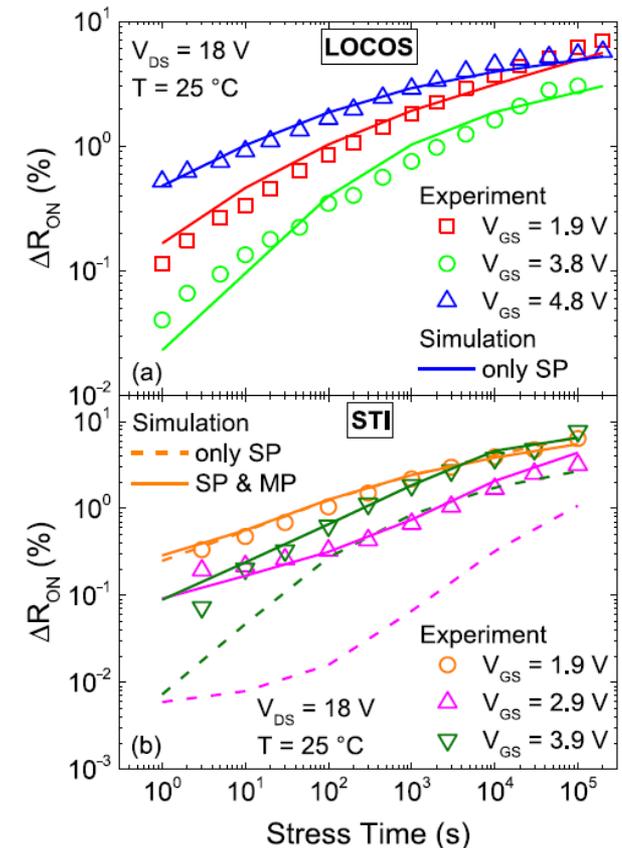
$$V_{OV} = 1 \text{ V}$$
$$V_{DS} = 18 \text{ V}$$



- A larger number of electrons is confined at the Si/SiO<sub>2</sub> interface of the STI architecture promoting **multiple-particle process**.

# Different Models Account for Different Architectures

- Single particle model seems more valid for previous generation architectures
- Multi particle model better fits with STI based architectures due to current closer confinement to the surface

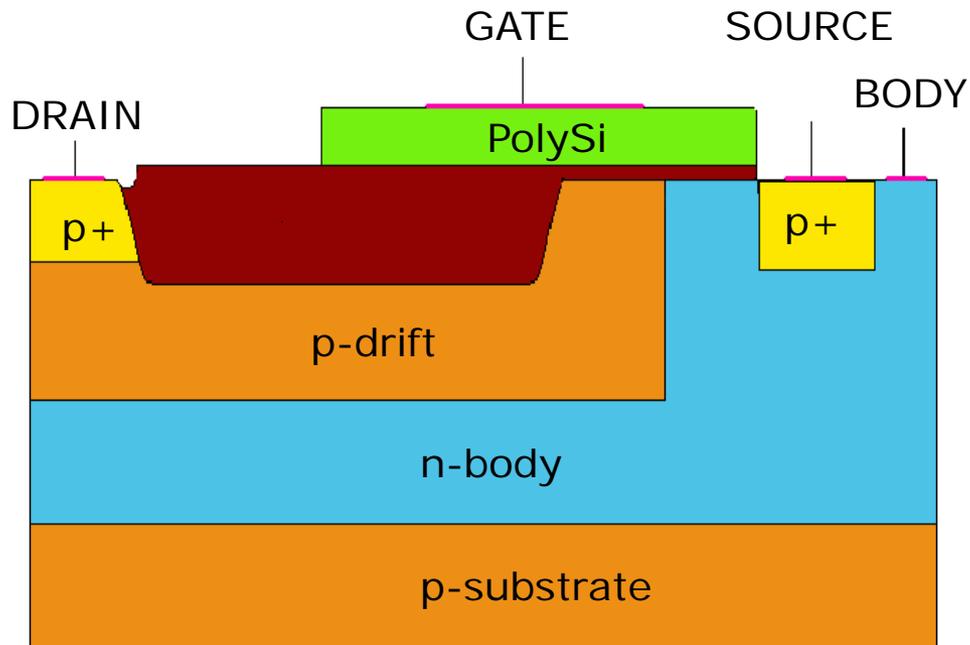


A. Tallarico et al., JEDS 2018

# Is the Methodology Always Valid?

- Can the tool be used also other components?
- Parameters work for both carriers?

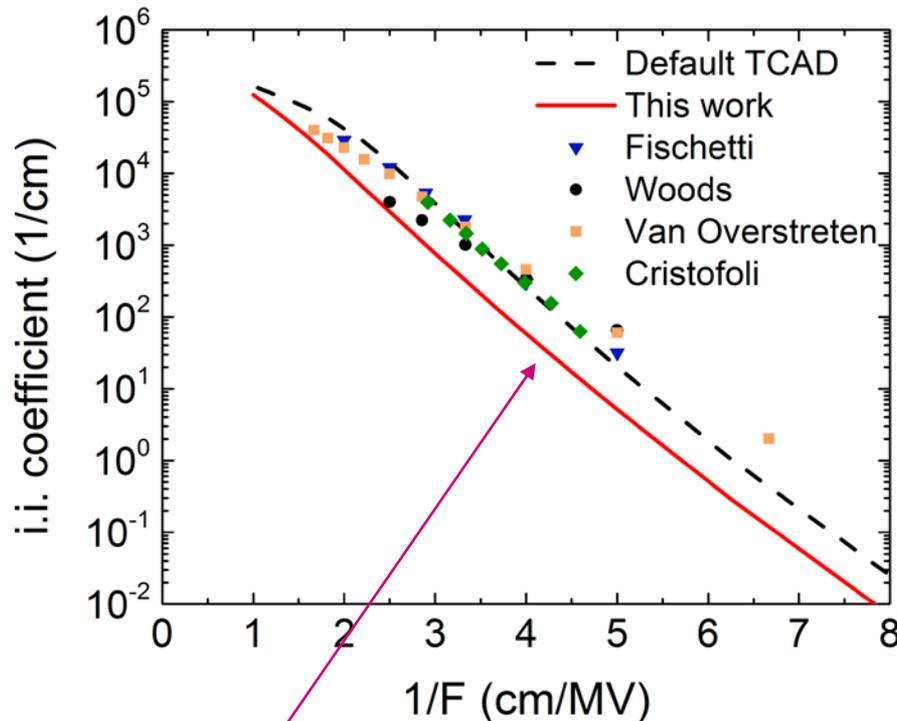
PCH structures must be considered



## HV p-channel LDMOS

- STI oxide structure
- Gate, body and drain currents analyzed

# Hole Avalanche Coefficient



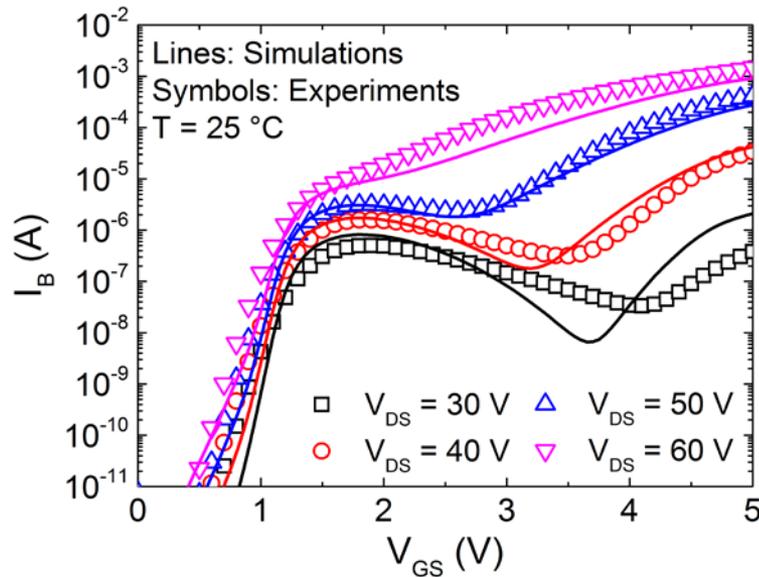
Reduction of the hole avalanche coefficient of about a factor 4 needed to reproduce the avalanche regime



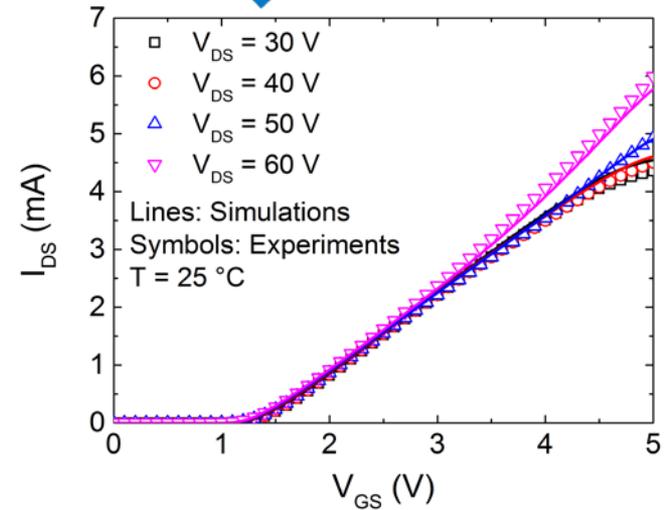
Parameters extrapolated from older technologies are no longer accurate for new generation technologies

F. Giuliano et al., ESSDERC 2019

# Body Current - PLDMOS



- $I_B - V_{GS}$  curves
- Turn on characteristics in saturation regime



Impact ionization peak at  $V_{GS}$  about 2V  
Body current decrease due to the reduction of the electric field

F. Giuliano et al., ESSDERC 2019

- An overview on some strategies to improve devices optimization devices robustness in mixed signal technologies was presented
- New and future technology process nodes must face the emerging of more stringent limitations in device operation due to the geometrical squizing
- TCAD tools will play a key role in trying to predict and help the device optimization going forward the classical breakdown and  $R_{on}$  optimization and speeding up the development phase

This work supported by:

ECSEL 2014-2-653933: R2POWER300 and H2020-EU ECSEL\_737417: R3-PowerUP

# Thank you for your attention