

# TCAD predictions of hot-electron injection in p-type LDMOS transistors

F. Giuliano<sup>a</sup>, A. N. Tallarico<sup>b</sup>, S. Reggiani<sup>a</sup>, A. Gnudi<sup>a</sup>, E. Sangiorgi<sup>b</sup>, C. Fiegna<sup>b</sup>, M. Rossetti<sup>c</sup>, A. Molfese<sup>c</sup>, S. Manzini<sup>c</sup>, R. Depetro<sup>c</sup>, G. Croce<sup>c</sup>

<sup>a</sup>University of Bologna (ARCES-DEI), Bologna, Italy <sup>b</sup>University of Bologna (ARCES-DEI), Cesena, Italy <sup>c</sup>STMicroelectronics, Agrate Brianza, Italy

> Work supported by H2020-EU ECSEL 737417: R3-PowerUP



### Outline



#### Introduction

- **□** Test structures and experiments
- **TCAD** analyses of the body current
- **TCAD** analysis of the gate current
- Conclusions

### Introduction



Device reliability for analog and high-voltage applications

Scaling of LDMOS

High field issues

Sources of device degradation



- Hot-carrier stress degradation
- Charge injection into gate oxide

# Introduction - Motivations



#### **P-type LDMOS transistors**



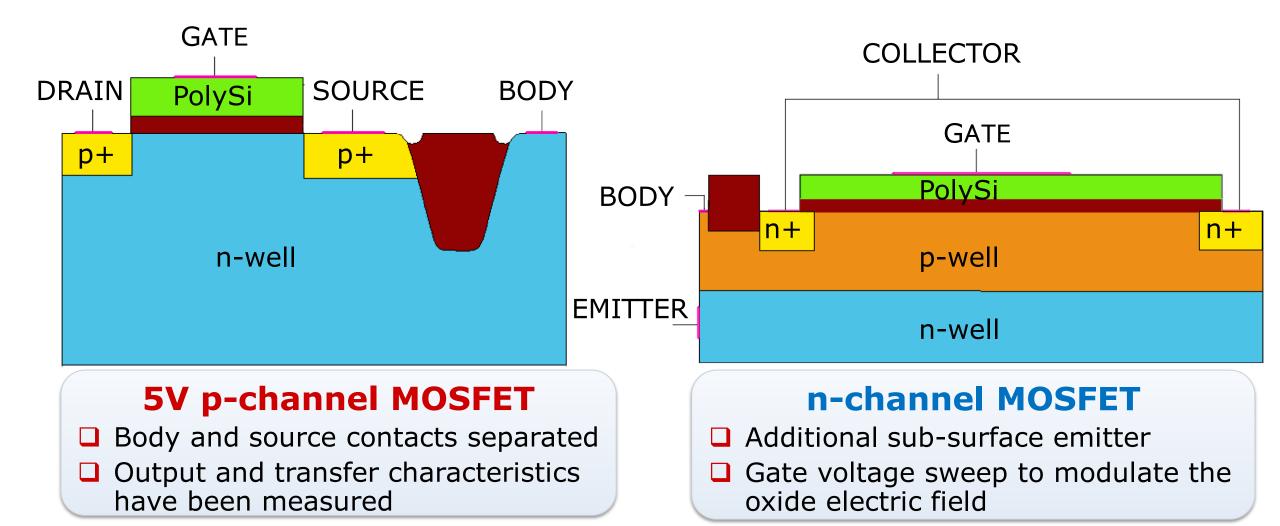
Hot carrier stress degradation: analyses on n-channel MOSFETs have shown that new nitrided Si/SiO<sub>2</sub> interfaces experience different features with respect to the old ones

 Hole impact-ionization coefficient still calibrated on very old experiments performed on bulk structures

TCAD investigation accounting for new characterization of:Electron injection probabilityHoles avalanche coefficient

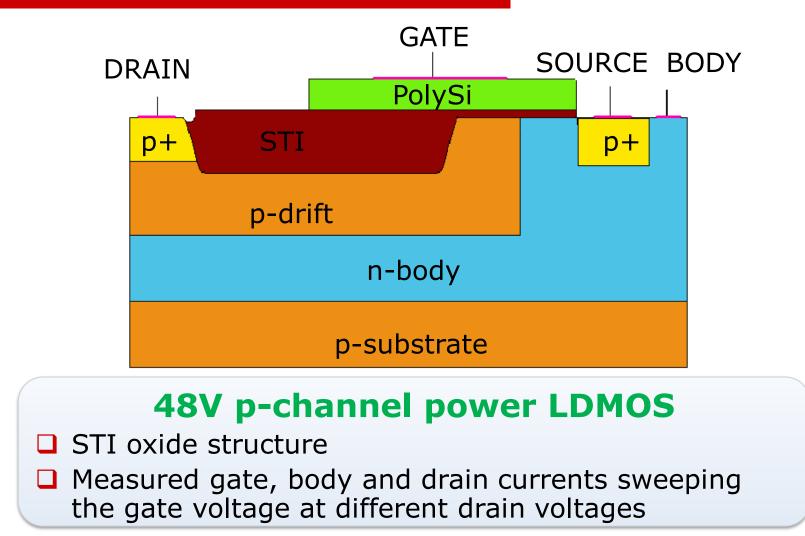


#### Test structures



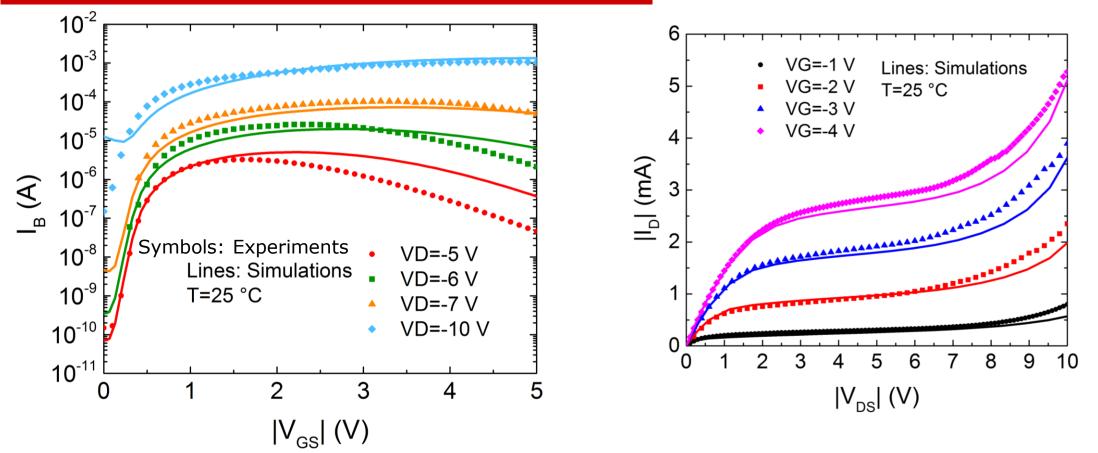


## Benchmark device





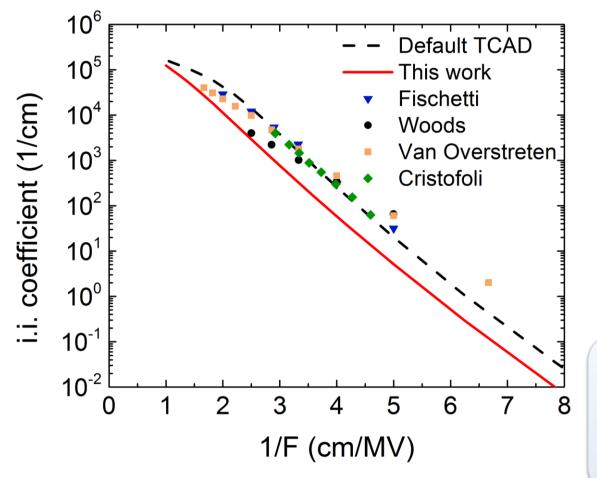
# Body current analysis - pMOSFET



- TCAD simulations using Unibo impact-ionization model
- □ I.i. coefficient tuned in order to fit  $I_B V_{GS}$  and  $I_D V_{DS}$  curves

# Hole avalanche coefficient





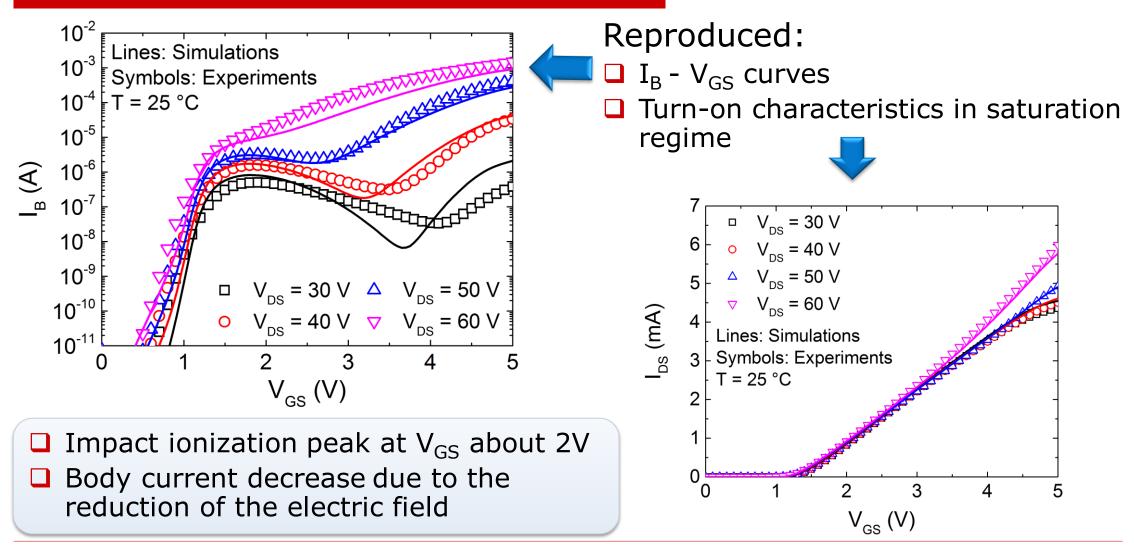
Reduction of the hole avalance coefficient of about a factor 4 to reproduce the avalanche regime



Parameters extrapolated from older technologies are no longer accurate for new generation technologies

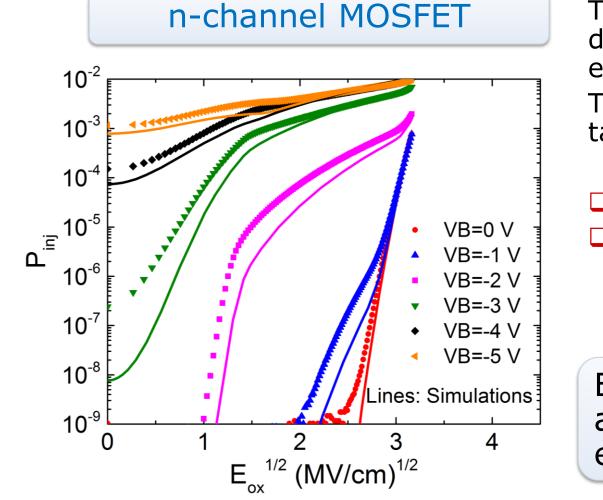
# Body current analysis - pLDMOS





# Electron injection probability





TCAD method based on the deterministic solution of the Boltzmann equation.

The implemented gate current model takes into account:

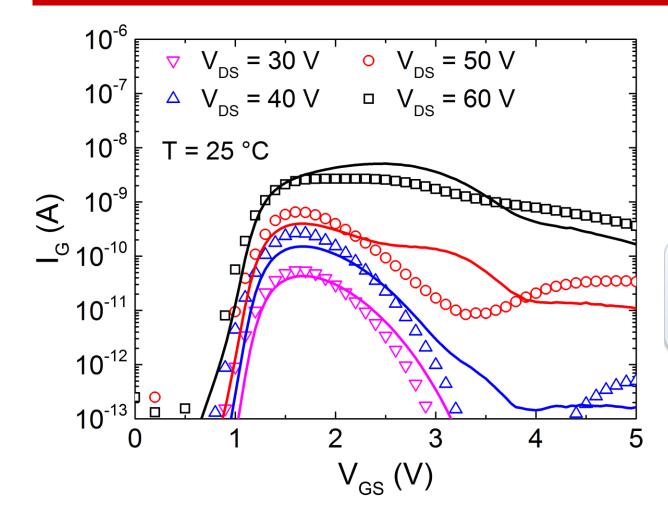
Tunneling component (low body bias)
Thermionic emission (high body bias)



Electron injection probabilities are accurately captured over an extended range of electric fields

# Gate current analysis





Same TCAD approach and parameters used to reproduce the  $I_G - V_{GS}$  characteristics of the **p-channel LDMOS transistor** 



Si/SiO<sub>2</sub> interface between the center of the STI and the drain excluded

Due to the Kirk effect, increasing the gate bias the location of the maximum impact ionization moves towards the drain region





- The role of hot electrons in a STI-based p-type LDMOS has been extensively investigated
- Calibration of TCAD models available in Synopsis TCAD tool against experiments on new generation structures
- Hole impact ionization and hot-electron injection mechanisms can be predicted in the case of p-channel power LDMOS transistors