Hot-Carrier Degradation in New Generation Power LDMOS: LOCOS- vs. STI-based Architecture

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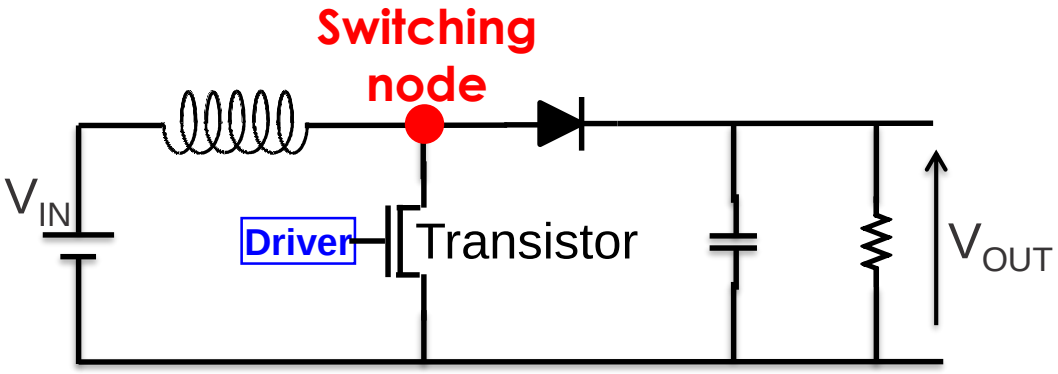
Outline

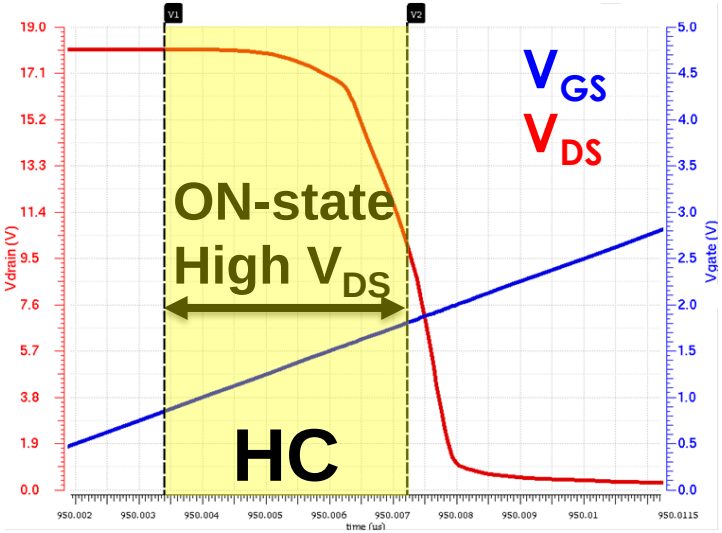
- **Introduction**
  - When hot-carrier degradation occurs in a real application
- **Devices description**
  - LOCOS vs. STI LDMOS transistors
- **Review of the Hot-Carrier Stress (HCS) degradation model**
- **Results and Discussion**
- **Conclusions**

Introduction

- HC degradation in a real application: **Switching phase**

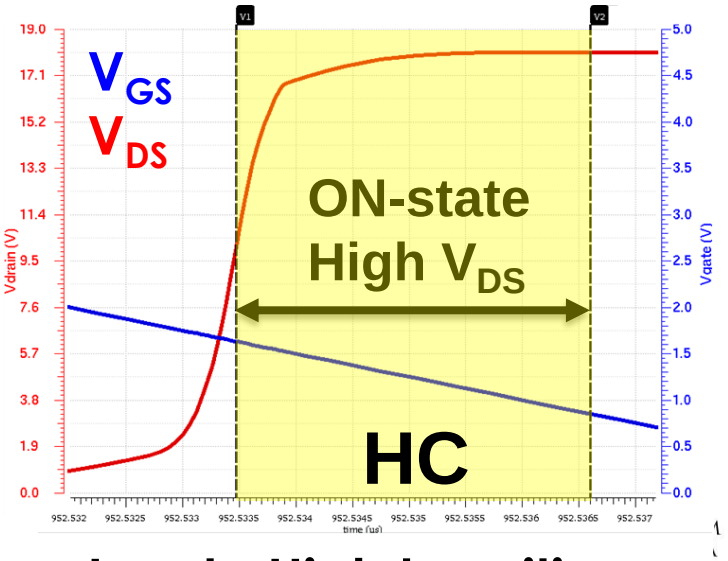
DC/DC boost converter





High to Low transition

Switching node simulation



Low to High transition

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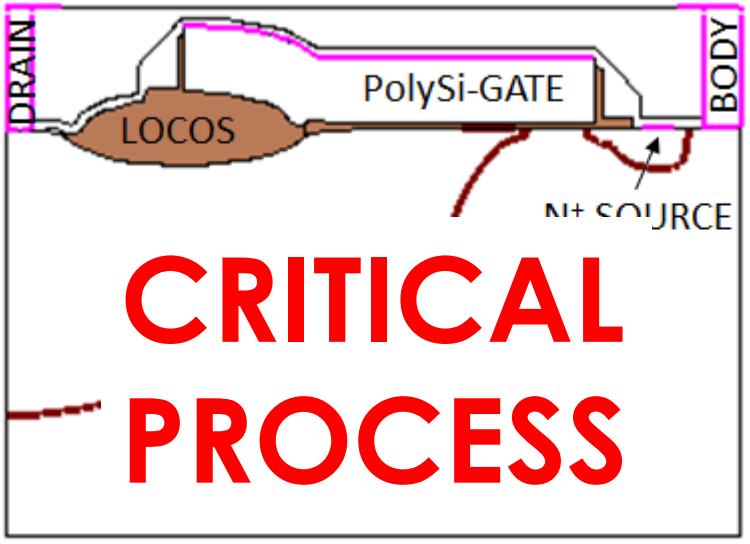
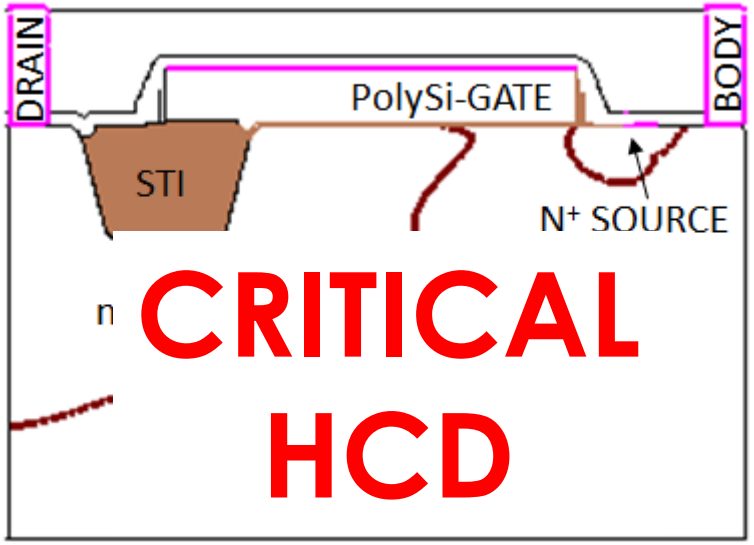
LDMOS structure: LOCOS vs STI

- N-drift LDMOS integrated in BCD technology
  - 200mm-wafer by STMicroelectronics
- Same Class voltage: 18 V
- Similar On-resistance: 8÷9 mΩ·mm^2
- Different threshold voltage: 0.85 V (LOCOS) and 1.4 V (STI)



LOCOS



STI

Purpose of this Work

- **To experimentally investigate** the hot-carrier degradation (HCD) in both LDMOS architectures
- **To reproduce** HCD by means of TCAD simulation
- **To understand** the main degradation mechanisms
- **To localize** the interface trap generation

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HCS Degradation Model

- TCAD model **developed** by S. Reggiani [1] and implemented in **Sentaurus simulator** [2] from 2016 version

- Different bond breakage mechanisms are included:
  - **Single-particle (SP)**, where a single hot particle is responsible;
  - **Multiple-particle (MP)**, where several colder carriers impinging the interface are responsible;
  - **Field-enhanced thermal (TH)**, where thermal interactions with the lattice are responsible.

[1] S. Reggiani, et al., T-ED, Vol. 60, No. 2, pp. 691-698, Feb. 2013
[2] Sentaurus-Device U.G. v. L-2016.03, Synopsys Inc., 2016

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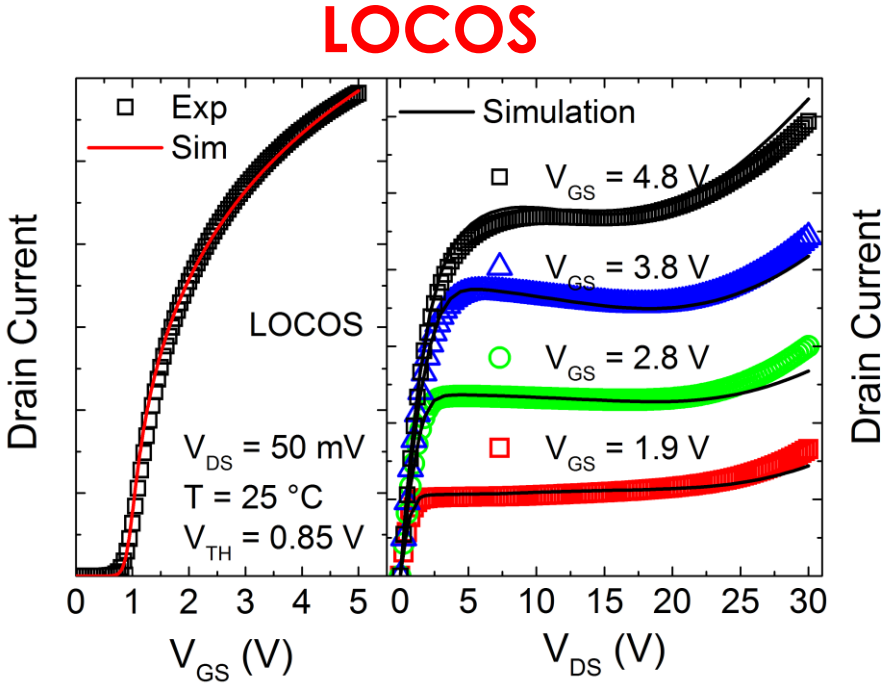
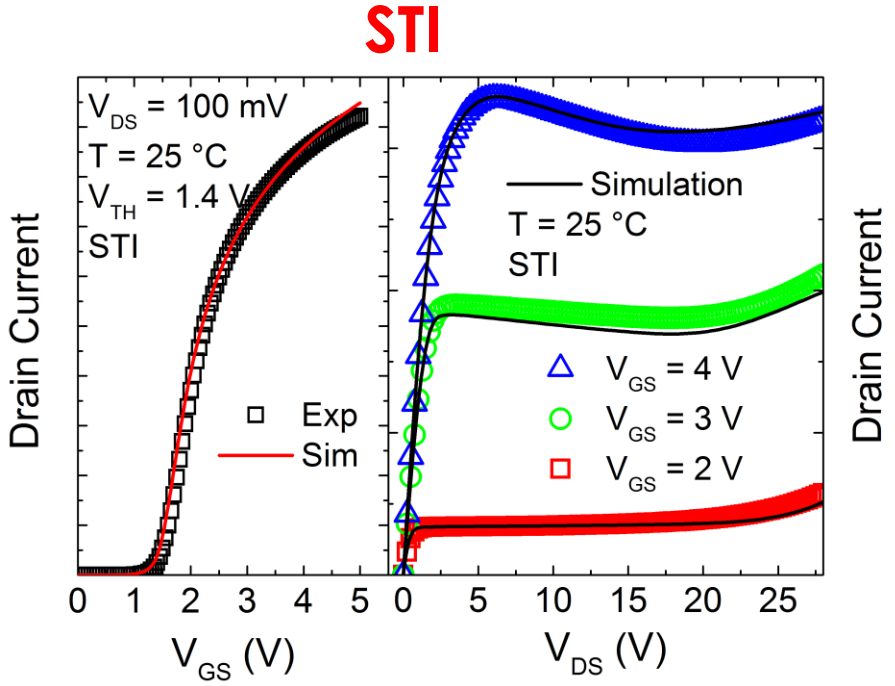
Device Calibration

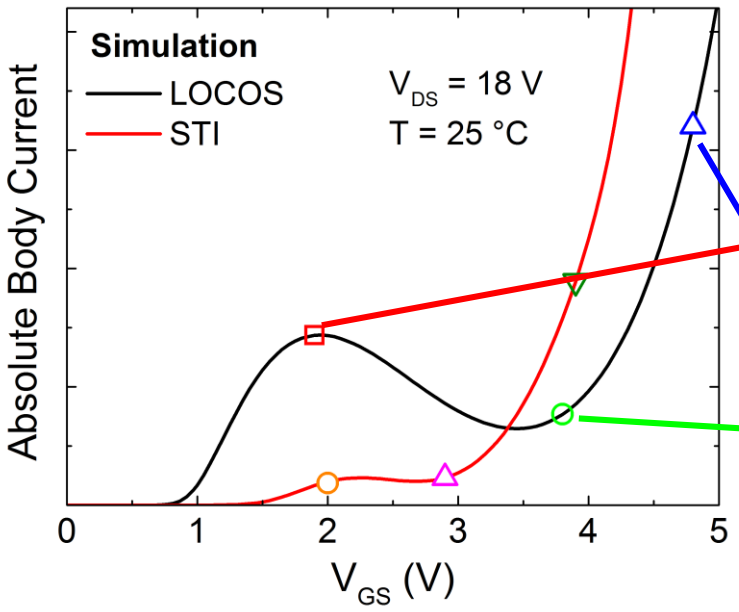
- TCAD calibration has been performed in order to reliably investigate the HC degradation

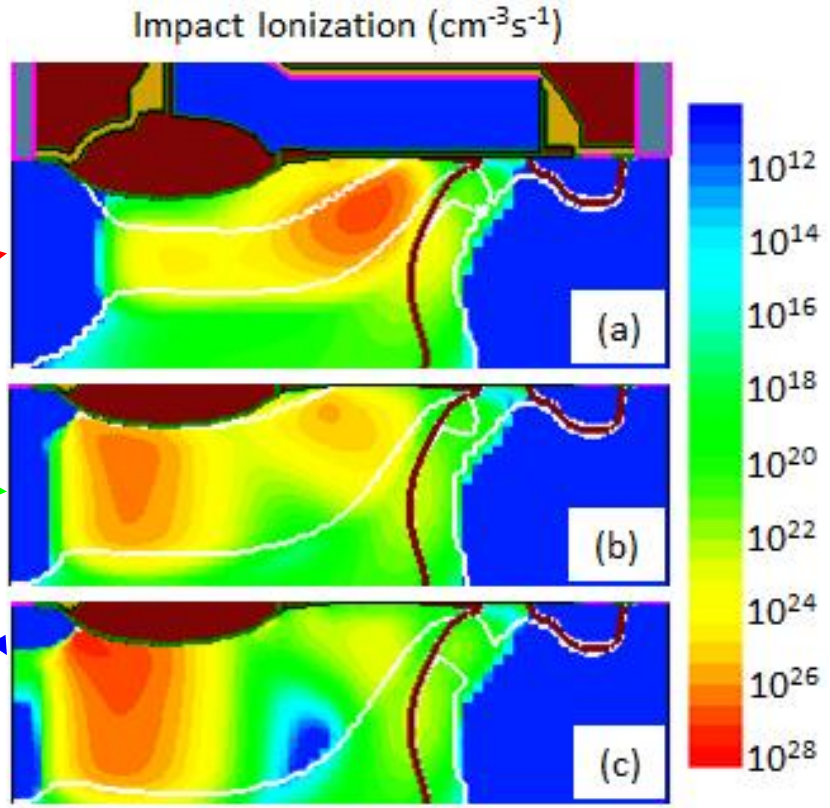




- Transfer, output, and off-state (not shown) characteristics accurately reproduced.

Identifying Hot Carrier Conditions

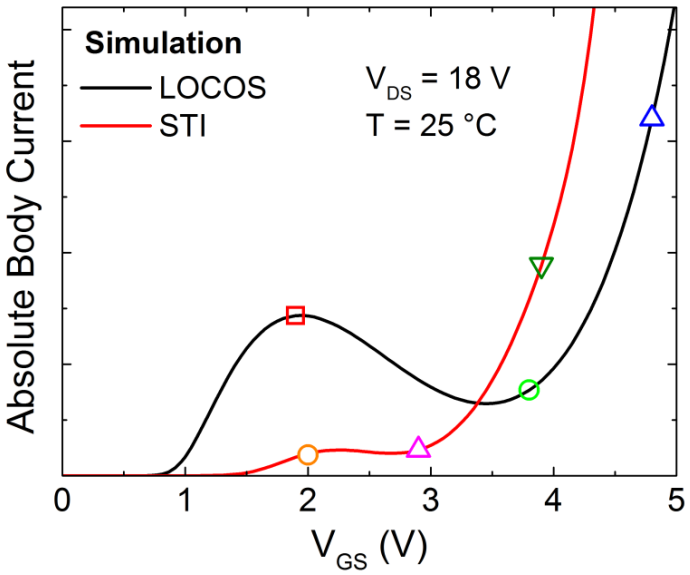


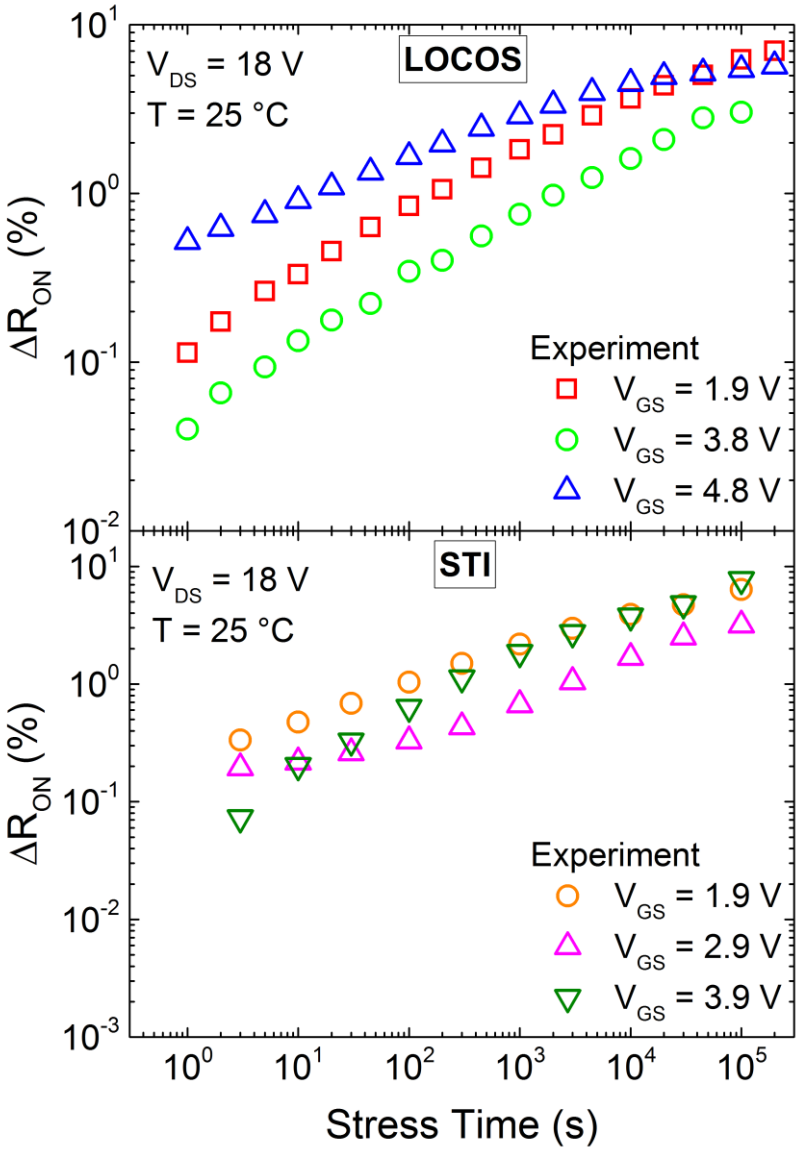


- Body current monitoring because of its correlation with the impact ionization (ii) generation;
- By increasing V_{GS} the ii peak moves towards the drain; I_B increases again due to Kirk effect;
- Same behavior observed in the STI structure (not shown);
- STI structure features a lower ii at relatively low V_{GS};

[3] A. N. Tallarico et al., Microelectronics Reliability, vol. 76-77, pp. 475-479, Sept. 2017

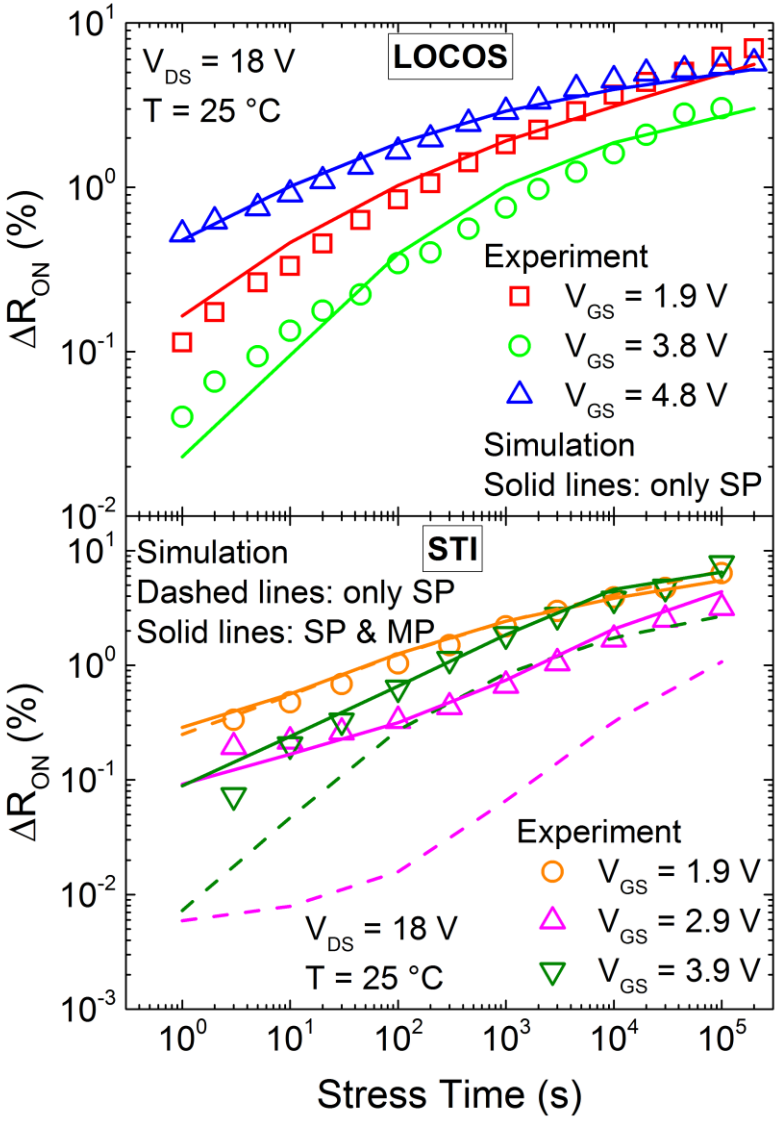
Body Current vs R_{ON} Degradation





- R_{ON} degradation perfectly follows body current in LOCOS devices
  - **Single-particle process** is the dominant degradation mechanism.
- No correlation in the case of STI devices
- Different degradation mechanisms occur in the two structures

R_{ON} Degradation (TCAD)

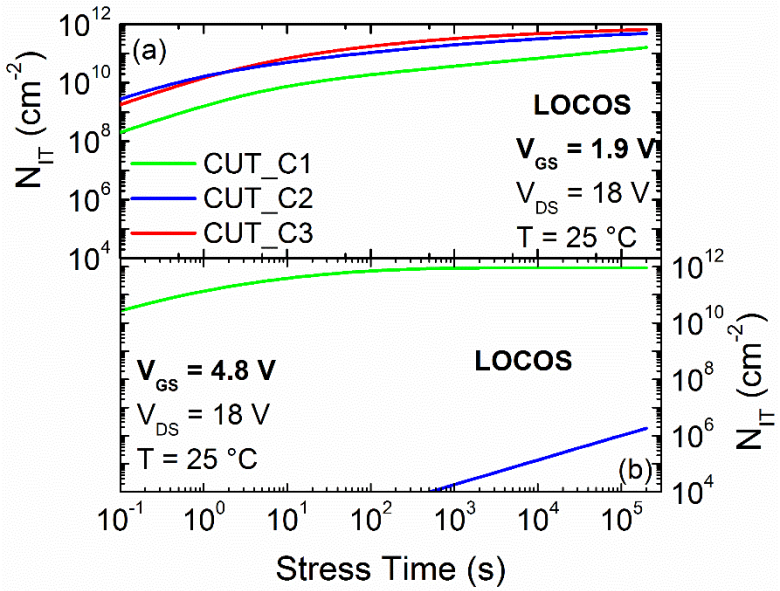


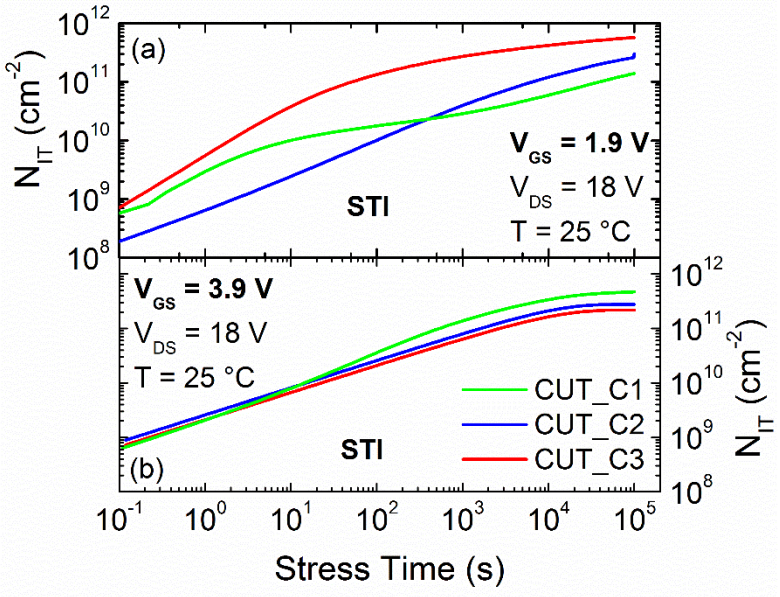
- **Single-particle** process is the **only enabled** degradation mechanism in the HCS model

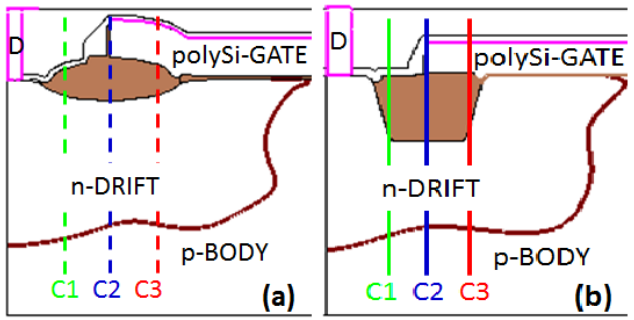
- Both **single-** and **multiple-particle** processes must be taken into account to reproduce experimental R_{ON} degradation

[4] A. N. Tallarico et al., IEEE JEDS, Vol. 6, no. 1, pp. 219-226, Jan. 2018

Where Degradation is Localized



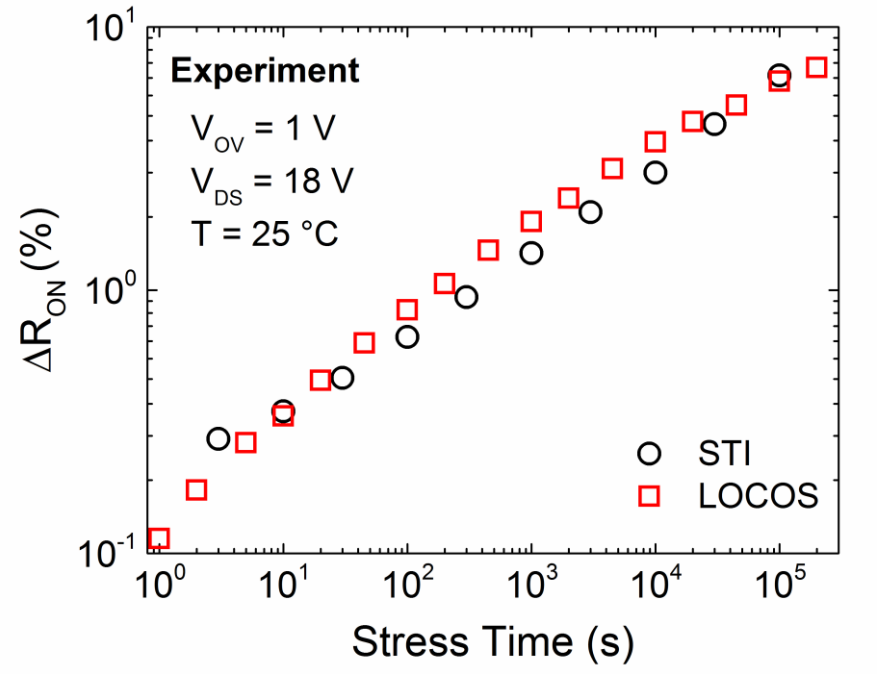


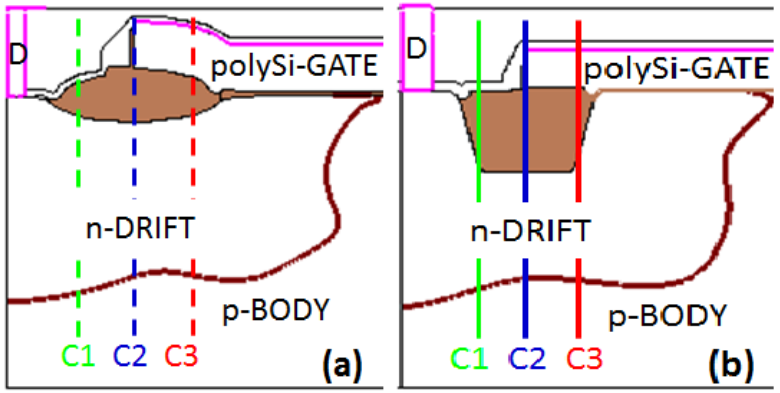


- At relatively low gate voltages, both devices show a higher trap generation at the source-side of the LOCOS/STI
- By increasing the gate voltage:
  - Interface trap generation in LOCOS follows the impact ionization peak, hence moves toward the drain contact;
  - In the case of STI, trap generation is uniformly distributed along the STI interface;

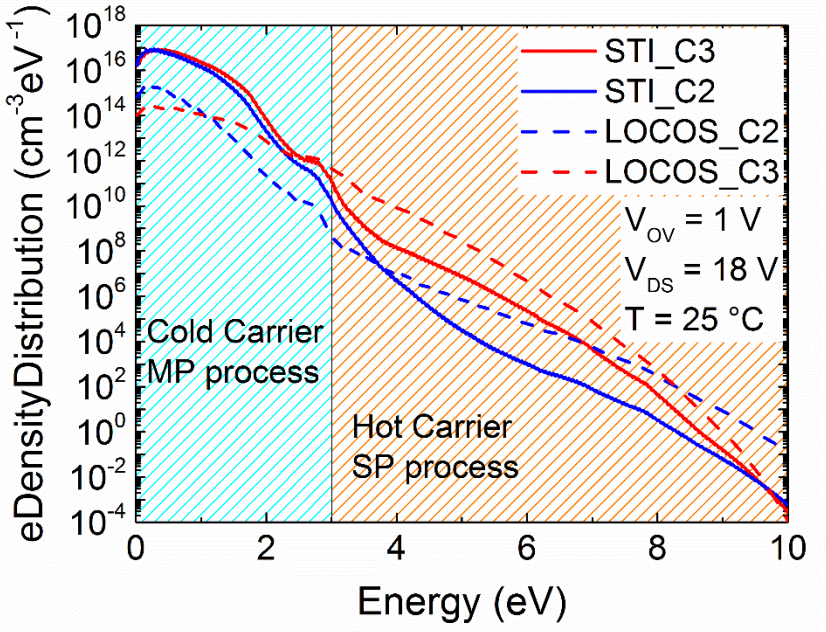
Direct Comparison: LOCOS vs STI

- Similar On-resistance degradation



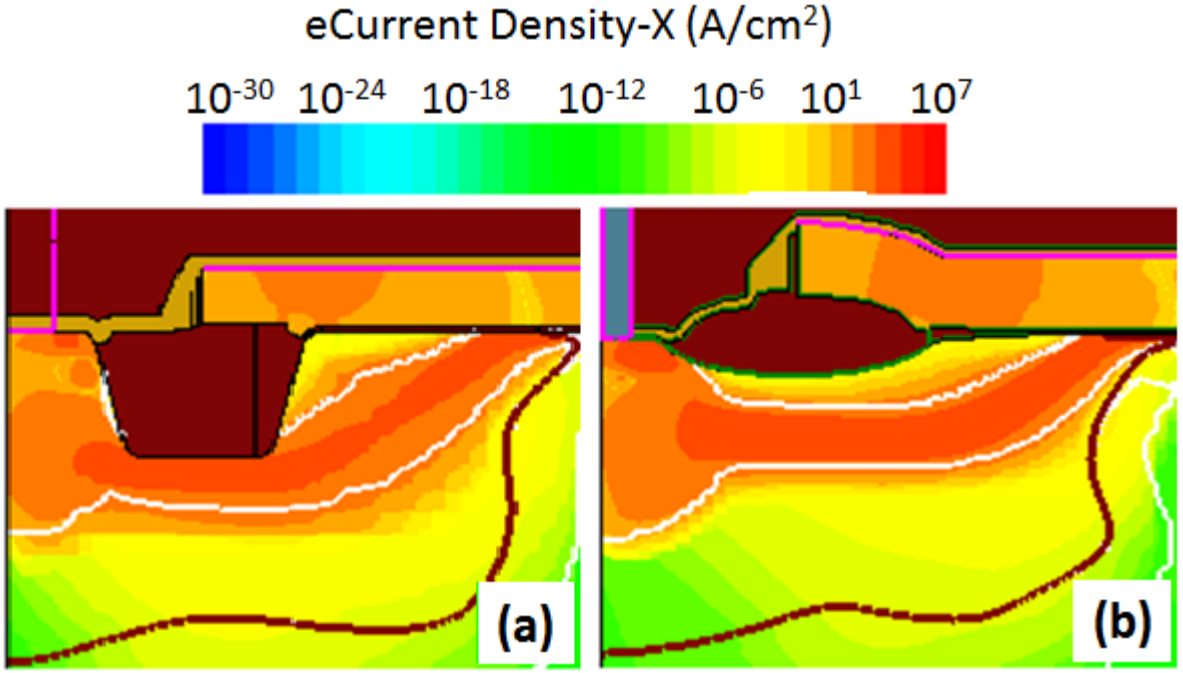


- STI: higher number of cold electrons
- LOCOS: higher number of hot carriers



Electron Current Density

Because of the etched trench (STI) deeper in silicon, the current flows confined at the interface of the STI bottom. As a result, a higher number of colder electrons interact with the molecules at the interface creating traps.



V_{OV} = 1 V
V_{DS} = 18 V
T = 25 °C

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Conclusions

- The two LDMOS architectures are affected by different HC degradation mechanisms: Single- and Multiple-particle;
- STI devices suffers from an additional degradation contribution due to multiple-cold-carriers caused by a deeper STI with respect to LOCOS;
- However, a clear reduction of the single high-energetic-carrier (reduced impact-ionization) due to the global result of different doping profiles and geometrical dimensions is attained in STI devices;
- Overall, STI devices are as robust as the LOCOS, guaranteeing same performance.

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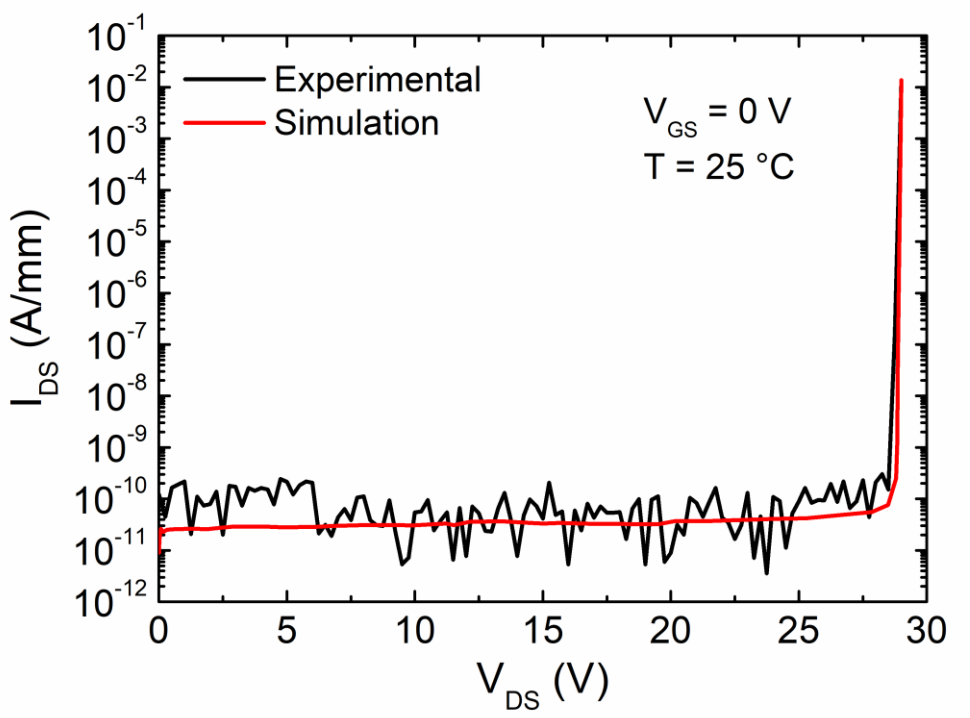
- ECSEL 2016-2-IA-737417:R3-PowerUP "300mm Pilot Line for Smart Power and Power Discrete"

Thank you for your attention

Appendix

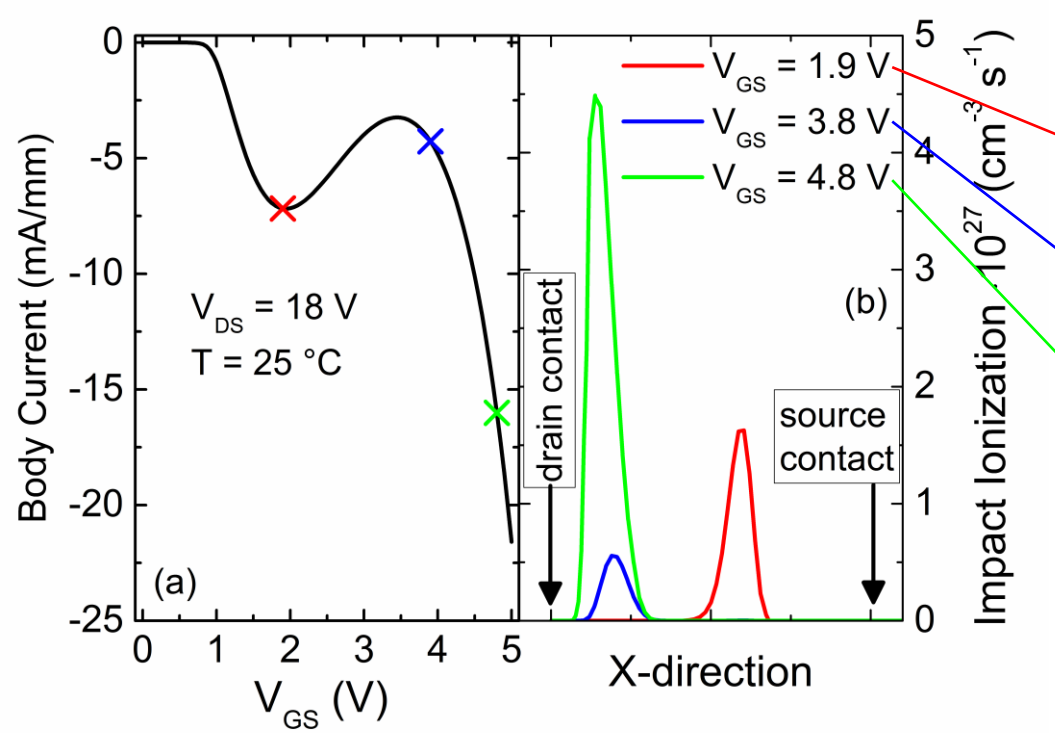
OFF-State Characteristics:LOCOS

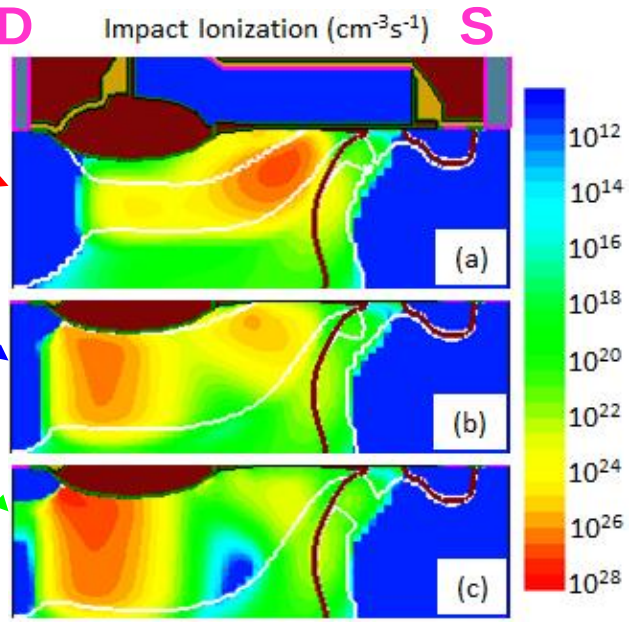
- Accurately reproduced by Sentaurus TCAD
  - van Overstraeten-de Man model



Body Current vs Impact Ionization

LOCOS





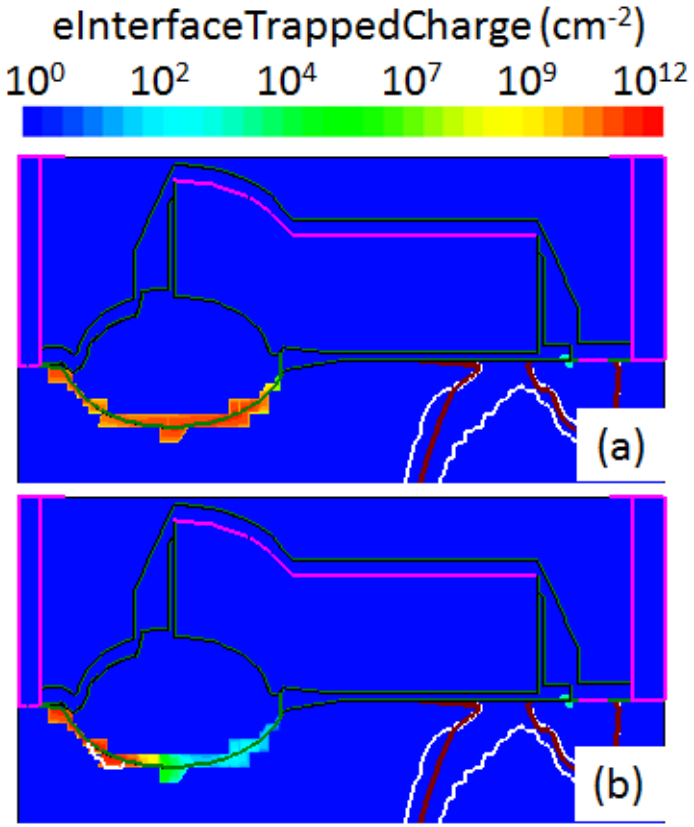
Spatial Interface Trap Distribution

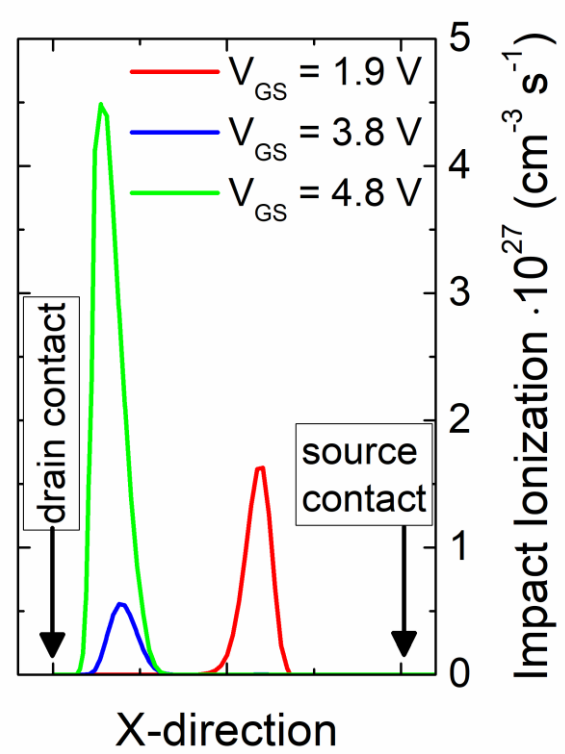
- By increasing the gate bias the impact ionization peak moves toward the drain creating defects at the silicon/oxide interface

V_{GS} = 1.9 V

DRAIN

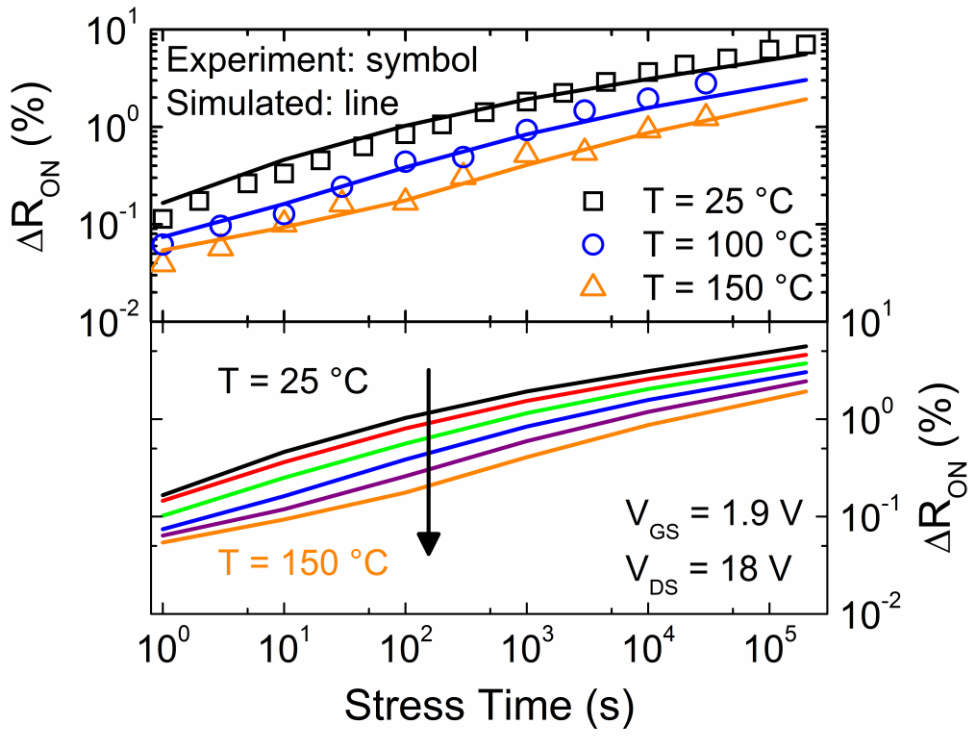
V_{GS} = 4.8 V





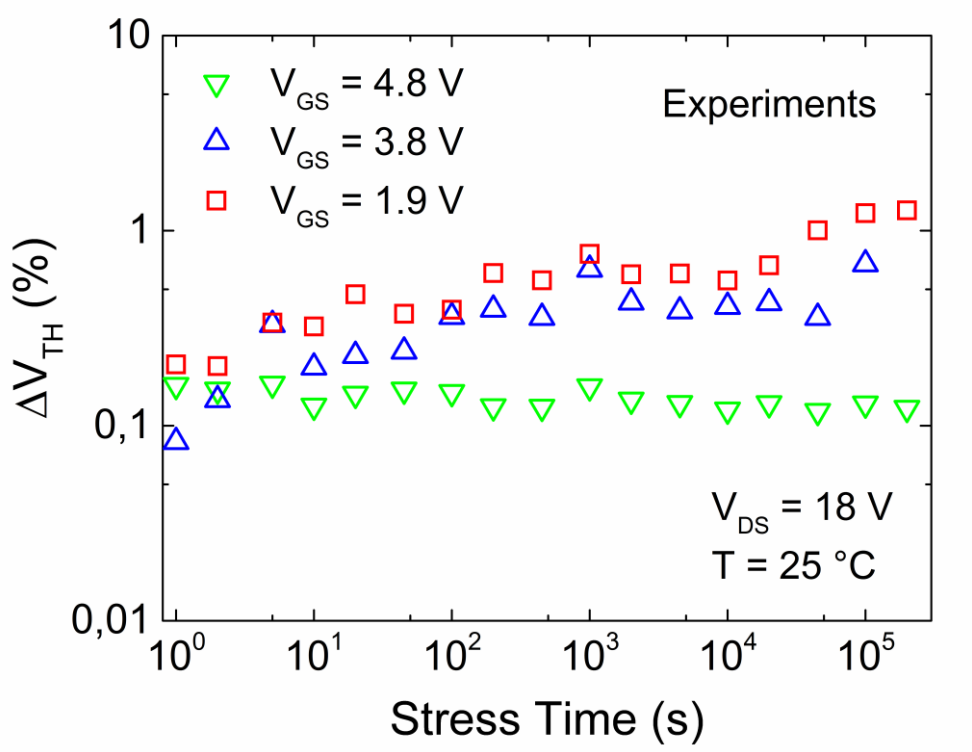
Temperature Dependence: LOCOS

- By increasing the temperature the ΔR_{ON} is reduced because of the phonon increase
  - the electron-phonon interactions tend to redistribute electrons from the high-energy tail to lower energies, thus reducing the HCS processes.



Threshold Voltage Degradation: LOCOS

- Negligible V_{TH} degradation is observed



HCS Degradation Model: SP

- **Interface trap density generated during hot-carrier**

$$N_{\mathrm{it,SP}}(\boldsymbol{r}, t, E_{\mathrm{SP}}) = P_{\mathrm{SP}} N_0 \left[1 - e^{-k_{\mathrm{SP}}(\boldsymbol{r}, E_{\mathrm{SP}})t}\right]$$

P_{SP}: probability for defect generation
N_0: maximum number of interface bonds
E_{SP}: activation energy for the SP process

- **Reaction rate for the SP process is given by the scattering-rate integral**

$$k_{\mathrm{SP}}(\boldsymbol{r}, E_{\mathrm{SP}}) = \int_{E_{\mathrm{SP}}}^{\infty} f(\boldsymbol{r}, E) g(E) v(E) \sigma_{\mathrm{SP}}(E) dE$$

f(r,E): carrier distribution function
g(E): total density of states
v(E): magnitude of carrier velocity

- **single-particle reaction cross-section**

$$\sigma_{\mathrm{SP}}(E) = \sigma_{\mathrm{SP0}} \left(\frac{E - E_{\mathrm{SP}}}{k_{\mathrm{B}} T}\right)^{p_{\mathrm{SP}}}$$

σ_{SP0}: fitting parameter
p_{sp}: exponent characterizing the SP process

[1] S. Reggiani, et al., T-ED, Vol. 60, No. 2, pp. 691-698, Feb. 2013
[2] Sentaurus-Device U.G. v. L-2016.03, Synopsys Inc., 2016

HCS Degradation Model: SP

- **Interface trap density generated during hot-carrier**

$$N_{\mathrm{it,MP}}(r, t, E_{\mathrm{MP}}) = P_{\mathrm{MP}} N_0 \left[\frac{P_{\mathrm{emi}}}{P_{\mathrm{pass}}} \left(\frac{P_{\mathrm{u}}}{P_{\mathrm{d}}} \right)^{N_1} (1 - e^{-P_{\mathrm{emi}} t}) \right]^{1/2}$$

P_{MP}: probability for defect generation
N_1: n° of energy levels in the oscillator that models the bond

- **Emission and passivation probabilities modelled as Arrhenius law**

$$P_{\mathrm{emi}} = \nu_{\mathrm{emi}} e^{-E_{\mathrm{emi}}/(k_{\mathrm{B}} T)}$$

$$P_{\mathrm{pass}} = \nu_{\mathrm{pass}} e^{-E_{\mathrm{pass}}/(k_{\mathrm{B}} T)}$$

V_{emi} and **V_{pass}** are the emission and passivation frequencies, respectively.
E_{emi} and **E_{pass}** are the emission and passivation energies, respectively.

- **Oscillator excitation and de-excitation probability**

$$P_{\mathrm{u}} = k_{\mathrm{ph}} e^{-E_{\mathrm{ph}}/(k_{\mathrm{B}} T)} + k_{\mathrm{MP}}(r, E_{\mathrm{MP}})$$

$$P_{\mathrm{d}} = k_{\mathrm{ph}} + k_{\mathrm{MP}}(r, E_{\mathrm{MP}})$$

E_{ph} and **k_{ph}** are the phonon energy and the reaction rate, respectively.
E_{MP} is the activation energy for MP processes.

[1] S. Reggiani, et al., T-ED, Vol. 60, No. 2, pp. 691-698, Feb. 2013
[2] Sentaurus-Device U.G. v. L-2016.03, Synopsys Inc., 2016

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